DDR3 SDRAM Registered DIMM
Based on 2Gb B-die

HMT325R7BFR8C
HMT351R7BFR8C
HMT351R7BFR4C
HMT31GR7BFR8C
HMT31GR7BFR4C
HMT42GR7BMR4C

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Jan.2010	Preliminary
0.2	Added IDD Specification	Feb.2010	
1.0	DIMM Outline Corrected	Jul.2010	
1.1	DIMM Outline Corrected	Aug.2010	
1.2	Added 1600 speed Supports	Nov.2010	
1.3	DIMM Outline Corrected	Dec.2010	
1.4	DIMM Outline Corrected	Dec.2011	
1.5	Latest JEDEC Spec and IDD Update	Mar.2012	

Description

Hynix Registered DDR3 SDRAM DIMMs (Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use Hynix DDR3 SDRAM devices. These Registered SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Features

- Power Supply: VDD=1.5V (1.425V to 1.575V)
- VDDQ = 1.5V (1.425V to 1.575V)
- VDDSPD=3.0V to 3.6V
- Functionality and operations comply with the DDR3L SDRAM datasheet
- 8 internal banks
- Data transfer rates: PC3-12800, PC3-10600, PC3-8500
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Supports ECC error correction and detection
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD
- This product is in compliance with the RoHS directive.

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks	FDHS
HMT325R7BFR8C-G7/H9/PB	2GB	256Mx72	256Mx8(H5TQ2G83BFR)*9	1	X
HMT351R7BFR8C-G7/H9/PB	4GB	512Mx72	256Mx8(H5TQ2G83BFR)*18	2	X
HMT351R7BFR4C-G7/H9/PB	4GB	512Mx72	512Mx4(H5TQ2G43BFR)*18	1	X
HMT31GR7BFR8C-G7/H9/PB	8GB	1Gx72	256Mx8(H5TQ2G83BFR)*36	4	O
HMT31GR7BFR4C-G7/H9/PB	8GB	1Gx72	512Mx4(H5TQ2G43BFR)*36	2	O
HMT42GR7BMR4C-G7/H9/PB	16GB	2Gx72	DDP 1Gx4(H5TQ4G43BMR)*36	4	O

* In order to uninstall FDHS, please contact sales administrator

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3-1066	-G7	1.875	7	13.125	13.125	37.5	50.625	7-7-7
DDR3-1333	-H9	1.5	9	13.5 (13.125)*	13.5 (13.125)*	36	49.5 (49.125)*	9-9-9
DDR3-1600	-PB	1.25	11	13.75 (13.125)*	13.75 (13.125)*	35	48.75 (48.125)*	11-11-11

*Hynix DRAM devices support optional downbinning to CL11, CL9, and CL7. SPD setting is programmed to match.

Speed Grade

Grade	Frequency [MHz]						Remark
	CL6	CL7	CL8	CL9	CL10	CL11	
-G7	800	1066	1066				
-H9	800	1066	1066	1333	1333		
-PB	800	1066	1066	1333	1333	1600	

Address Table

	2GB(1Rx8)	4GB(2Rx8)	4GB(1Rx4)	8GB(4Rx8)	8GB(2Rx4)	16GB(4Rx4)
Refresh Method	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms
Row Address	A0-A13	A0-A13	A0-A13	A0-A13	A0-A13	A0-A13
Column Address	A0-A9	A0-A9	A0-A9,A11	A0-A9	A0-A9,A11	A0-A9,A11
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2
Page Size	1KB	1KB	1KB	1KB	1KB	1KB

Pin Descriptions

Pin Name	Description	Num ber	Pin Name	Description	Num ber
CK0	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
$\overline{\text{CK0}}$	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CK1	Clock Input, positive line	1	CB[7:0]	Data check bits Input/Output	8
$\overline{\text{CK1}}$	Clock Input, negative line	1	DQS[8:0]	Data strobes	9
CKE[1:0]	Clock Enables	2	$\overline{\text{DQS[8:0]}}$	Data strobes, negative line	9
$\overline{\text{RAS}}$	Row Address Strobe	1	DM[8:0]/ DQS[17:9], TDQS[17:9]	Data Masks / Data strobes, Termination data strobes	9
$\overline{\text{CAS}}$	Column Address Strobe	1	$\overline{\text{DQS[17:9]}}$, $\overline{\text{TDQS[17:9]}}$	Data strobes, negative line, Termination data strobes	9
$\overline{\text{WE}}$	Write Enable	1	$\overline{\text{EVENT}}$	Reserved for optional hardware temperature sensing	1
$\overline{\text{S[3:0]}}$	Chip Selects	4	TEST	Memory bus test tool (Not Connected and Not Usable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	$\overline{\text{RESET}}$	Register and SDRAM control pin	1
A10/AP	Address Input/Autoprecharge	1	V_{DD}	Power Supply	22
A12/$\overline{\text{BC}}$	Address Input/Burst chop	1	V_{SS}	Ground	59
BA[2:0]	SDRAM Bank Addresses	3	V_{REFDQ}	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{REFCA}	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	V_{TT}	Termination Voltage	4
SA[2:0]	SPD Address Inputs	3	V_{DDSPD}	SPD Power	1
Par_In	Parity bit for the Address and Control bus	1			
$\overline{\text{Err_Out}}$	Parity error found on the Address and Control bus	1			

Input/Output Functional Descriptions

Symbol	Type	Polarity	Function
CK0	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
$\overline{\text{CK0}}$	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1	IN	Positive Line	Terminated but not used on RDIMMs.
$\overline{\text{CK1}}$	IN	Negative Line	Terminated but not used on RDIMMs.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{\text{S[3:0]}}$	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, $\overline{\text{S[3:2]}}$ operate similarly to $\overline{\text{S[1:0]}}$ for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
V_{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V_{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{S0}}$, $\overline{\text{S1}}$, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle.
A[15:13, 12/$\overline{\text{BC}}$,11, 10/AP,[9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during $\overline{\text{CAS}}$ command. The address inputs also provide the op-code during Mode Register Set commands.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V_{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.

Symbol	Type	Polarity	Function
DQS[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
$\overline{\text{DQS[17:0]}}$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
TDQS[17:9] $\overline{\text{TDQS[17:9]}}$	OUT		TDQS/$\overline{\text{TDQS}}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1,DRAM will enable the same termination resistance function on TDQS/$\overline{\text{TDQS}}$ that is applied to DQS/$\overline{\text{DQS}}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and $\overline{\text{TDQS}}$ is not used. X4 DRAMs must disable the TDQS function via mode register A11=0 in MR1
SA[2:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
$\overline{\text{EVENT}}$	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{\text{EVENT}}$ pin on TS/SPD part. No pull-up resister is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
$\overline{\text{RESET}}$	IN		The $\overline{\text{RESET}}$ pin is connected to the $\overline{\text{RESET}}$ pin on the register and to the $\overline{\text{RESET}}$ pin on the DRAM.
Par_In	IN		Parity bit for the Address and Control bus. (“1 “: Odd, “0 “: Even)
$\overline{\text{Err_Out}}$	OUT (open drain)		Parity error detected on the Address and Control bus. A resistor may be connected from $\overline{\text{Err_Out}}$ bus line to V_{DD} on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Pin Assignments

Pin #	Front Side (left 1–60)	Pin #	Back Side (right 121–180)	Pin #	Front Side (left 61–120)	Pin #	Back Side (right 181–240)
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	DQ4	62	VDD	182	VDD
3	DQ0	123	DQ5	63	NC, CK1	183	VDD
4	DQ1	124	VSS	64	NC, $\overline{\text{CK1}}$	184	CK0
5	VSS	125	DM0,DQS9, TDQS9	65	VDD	185	$\overline{\text{CK0}}$
6	$\overline{\text{DQS0}}$	126	NC,$\overline{\text{DQS9}}$, $\overline{\text{TDQS9}}$	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	$\overline{\text{EVENT}}$, NC
8	VSS	128	DQ6	68	Par_In, NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10 / AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	$\overline{\text{RAS}}$
13	DQ9	133	VSS	73	$\overline{\text{WE}}$	193	$\overline{\text{S0}}$
14	VSS	134	DM1,DQS10, TDQS10	74	$\overline{\text{CAS}}$	194	VDD
15	$\overline{\text{DQS1}}$	135	NC,$\overline{\text{DQS10}}$, $\overline{\text{TDQS10}}$	75	VDD	195	ODT0
16	DQS1	136	VSS	76	$\overline{\text{S1}}$, NC	196	A13
17	VSS	137	DQ14	77	ODT1, NC	197	VDD
18	DQ10	138	DQ15	78	VDD	198	$\overline{\text{S3}}$, NC
19	DQ11	139	VSS	79	$\overline{\text{S2}}$, NC	199	VSS
20	VSS	140	DQ20	80	VSS	200	DQ36
21	DQ16	141	DQ21	81	DQ32	201	DQ37
22	DQ17	142	VSS	82	DQ33	202	VSS
23	VSS	143	DM2,DQS11, TDQS11	83	VSS	203	DM4,DQS13, TDQS13
24	$\overline{\text{DQS2}}$	144	NC,$\overline{\text{DQS11}}$, $\overline{\text{TDQS11}}$	84	$\overline{\text{DQS4}}$	204	NC,$\overline{\text{DQS13}}$, $\overline{\text{TDQS13}}$
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	DQ22	86	VSS	206	DQ38
27	DQ18	147	DQ23	87	DQ34	207	DQ39
28	DQ19	148	VSS	88	DQ35	208	VSS
29	VSS	149	DQ28	89	VSS	209	DQ44
30	DQ24	150	DQ29	90	DQ40	210	DQ45
31	DQ25	151	VSS	91	DQ41	211	VSS

NC = No Connect; RFU = Reserved Future Use

Pin #	Front Side (left 1–60)	Pin #	Back Side (right 121–180)	Pin #	Front Side (left 61–120)	Pin #	Back Side (right 181–240)
32	VSS	152	DM3,DQS12, TDQS12	92	VSS	212	DM5,DQS14, TDQS14
33	$\overline{\text{DQS3}}$	153	NC,$\overline{\text{DQS12}}$, $\overline{\text{TDQS12}}$	93	$\overline{\text{DQS5}}$	213	NC,$\overline{\text{DQS14}}$, $\overline{\text{TDQS14}}$
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	DQ30	95	VSS	215	DQ46
36	DQ26	156	DQ31	96	DQ42	216	DQ47
37	DQ27	157	VSS	97	DQ43	217	VSS
38	VSS	158	CB4, NC	98	VSS	218	DQ52
39	CB0, NC	159	CB5, NC	99	DQ48	219	DQ53
40	CB1, NC	160	VSS	100	DQ49	220	VSS
41	VSS	161	NC,DM8,DQS17, TDQS17	101	VSS	221	DM6,DQS15, TDQS15
42	$\overline{\text{DQS8}}$	162	NC,$\overline{\text{DQS17}}$, $\overline{\text{TDQS17}}$	102	$\overline{\text{DQS6}}$	222	NC,$\overline{\text{DQS15}}$, $\overline{\text{TDQS15}}$
43	DQS8	163	VSS	103	DQS6	223	VSS
44	VSS	164	CB6, NC	104	VSS	224	DQ54
45	CB2, NC	165	CB7, NC	105	DQ50	225	DQ55
46	CB3, NC	166	VSS	106	DQ51	226	VSS
47	VSS	167	NC(TEST)	107	VSS	227	DQ60
48	VTT, NC	168	$\overline{\text{RESET}}$	108	DQ56	228	DQ61
KEY		KEY		109	DQ57	229	VSS
49	VTT, NC	169	CKE1, NC	110	VSS	230	DM7,DQS16, TDQS16
50	CKE0	170	VDD	111	$\overline{\text{DQS7}}$	231	NC,$\overline{\text{DQS16}}$, $\overline{\text{TDQS16}}$
51	VDD	171	A15	112	DQS7	232	VSS
52	BA2	172	A14	113	VSS	233	DQ62
53	$\overline{\text{Err_Out}}$, NC	173	VDD	114	DQ58	234	DQ63
54	VDD	174	A12 / $\overline{\text{BC}}$	115	DQ59	235	VSS
55	A11	175	A9	116	VSS	236	VDDSPD
56	A7	176	VDD	117	SA0	237	SA1
57	VDD	177	A8	118	SCL	238	SDA
58	A5	178	A6	119	SA2	239	VSS
59	A4	179	VDD	120	VTT	240	VTT
60	VDD	180	A3				

NC = No Connect; RFU = Reserved Future Use

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Registering Clock Driver Specifications

Capacitance Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input capacitance, Data inputs		1.5	-	2.5	pF
	Input capacitance, CK, $\overline{CK}$, FBIN, $\overline{FBIN}$ (up to DDR3-1600)		1.5	-	2.5	pF
C_{IR}	Input capacitance, $\overline{RESET}$, MIRROR, QCSEN	$V_I = V_{DD}$ or GND; $V_{DD} = 1.5v$	-	-	3	pF

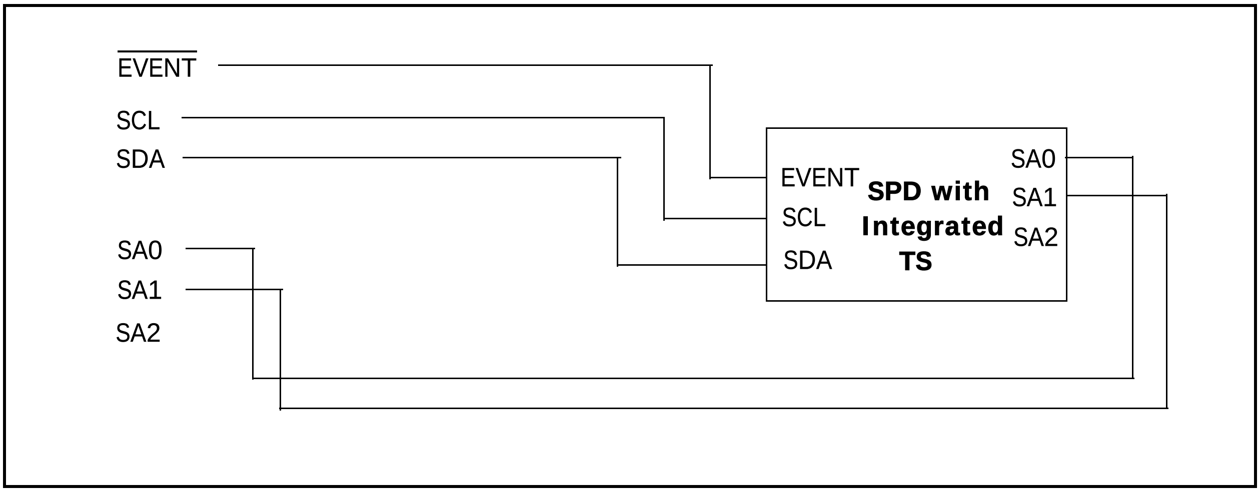
Input & Output Timing Requirements

Symbol	Parameter	Conditions	DDR3-800 1066/1333		DDR3-1600		Unit
			Min	Max	Min	Max	
f_{clock}	Input clock frequency	Application frequency	300	670	300	810	Mhz
f_{TEST}	Input clock frequency	Test frequency	70	300	70	300	Mhz
t_{SU}	Setup time	Input valid before CK/$\overline{CK}$	100	-	50	-	ps
t_H	Hold time	Input to remain valid after CK/$\overline{CK}$	175	-	125	-	ps
t_{PDM}	Propagation delay, single-bit switching	CK/$\overline{CK}$ to output	0.65	1.0	0.65	1.0	ns
t_{DIS}	Output disable time (1/2-Clock prelaunch)	Yn/$\overline{Yn}$ to output float	0.5 + tQSK1(min)	-	0.5 + tQSK1(min)	-	ps
t_{EN}	Output enable time (1/2-Clock prelaunch)	Output driving to Yn/$\overline{Yn}$	0.5 - tQSK1(max)	-	0.5 - tQSK1(max)	-	ps

On DIMM Thermal Sensor

The DDR3 SDRAM DIMM temperature is monitored by integrated thermal sensor. The integrated thermal sensor comply with JEDEC “TSE2002av, Serial Presence Detect with Temperature Sensor”.

Connection of Thermal Sensor

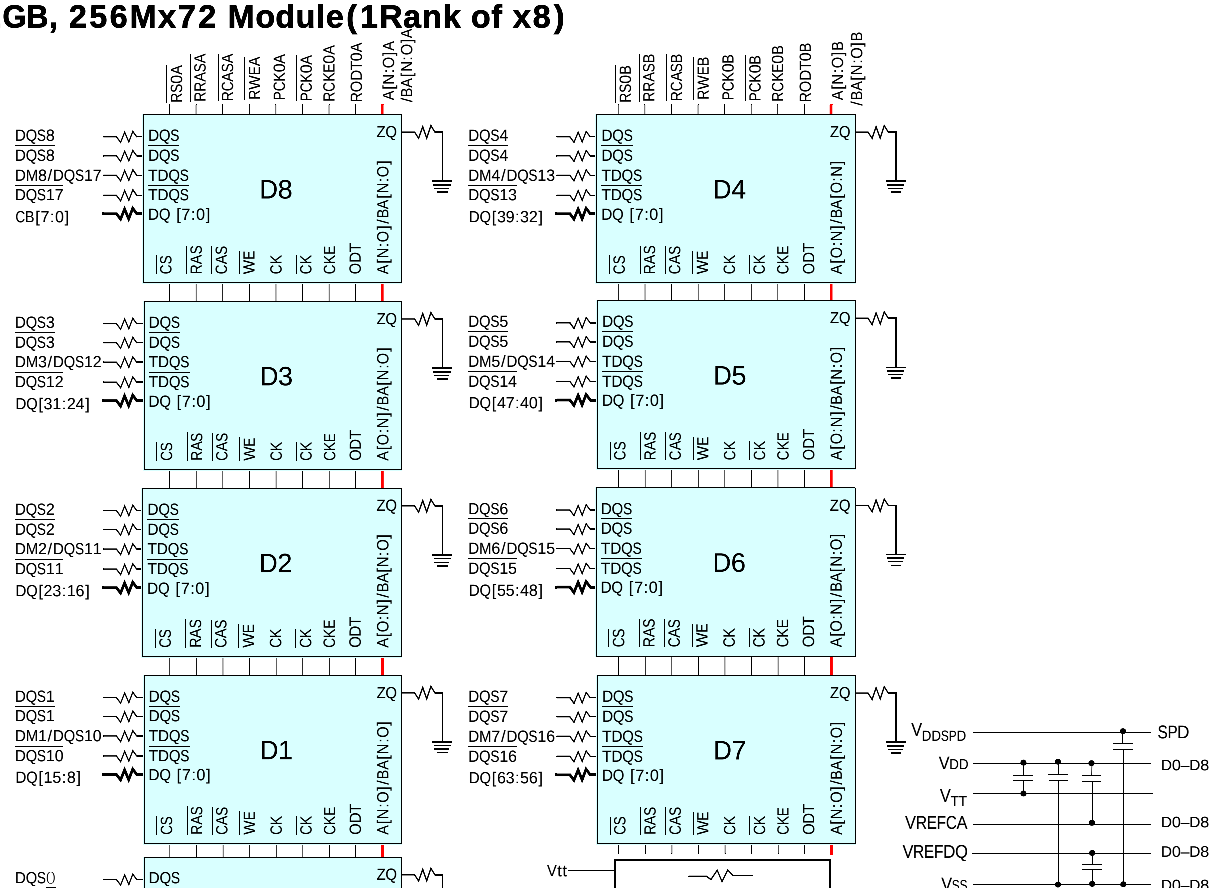


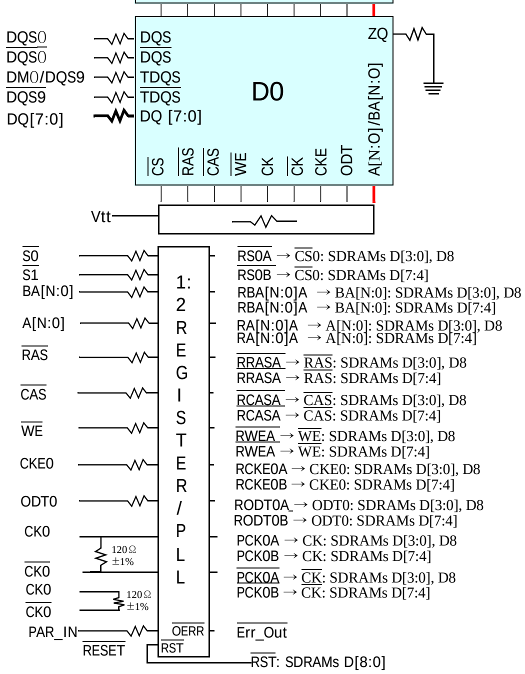
Temperature-to-Digital Conversion Performance

Parameter	Condition	Min	Typ	Max	Unit
Temperature Sensor Accuracy (Grade B)	Active Range, 75°C < T_A < 95°C	-	± 0.5	± 1.0	°C
	Monitor Range, 40°C < T_A < 125°C	-	± 1.0	± 2.0	°C
	-20°C < T_A < 125°C	-	± 2.0	± 3.0	°C
Resolution			0.25		°C

Functional Block Diagram

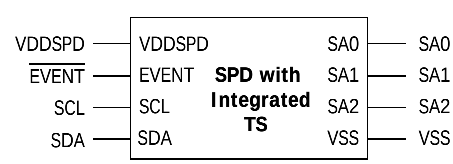
2GB, 256Mx72 Module(1Rank of x8)





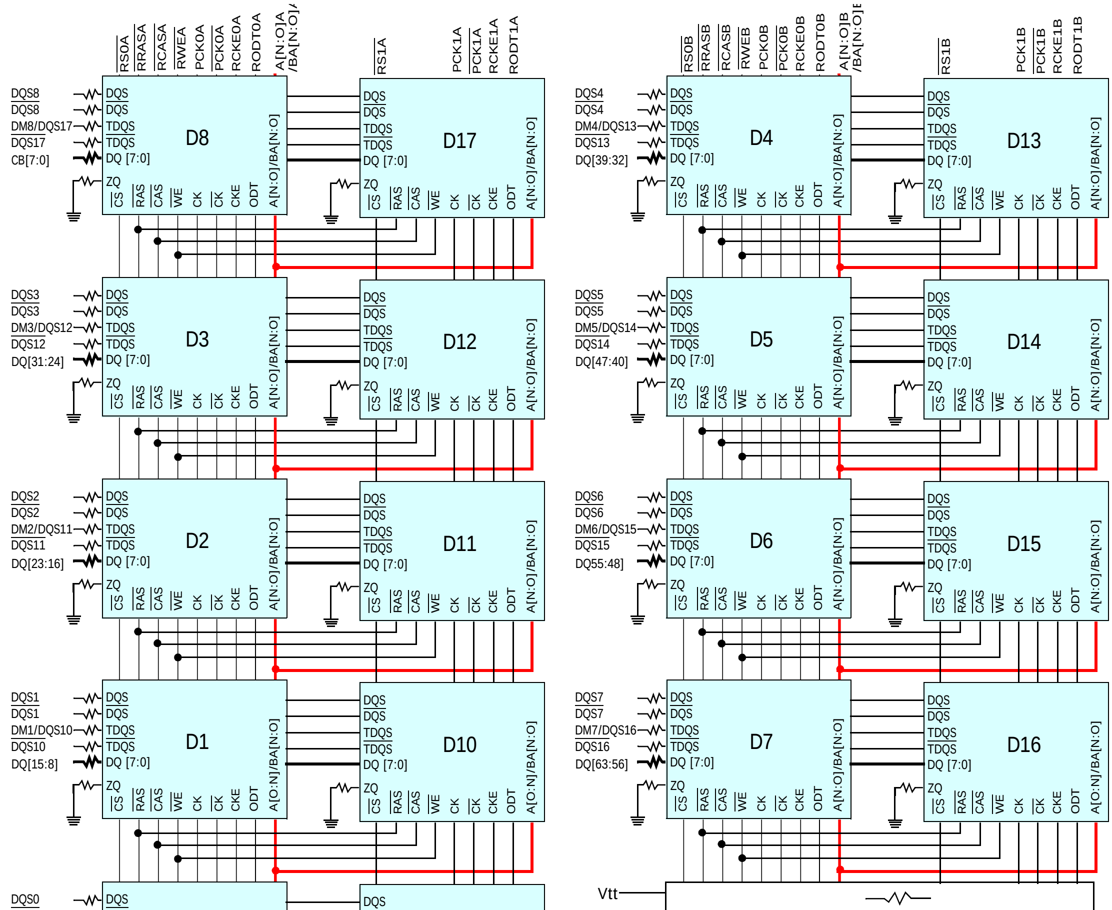
S[3:2], CKE1, ODT1, are NC (Unused register inputs ODT1 and CKE1 have a 330Ω resistor to ground

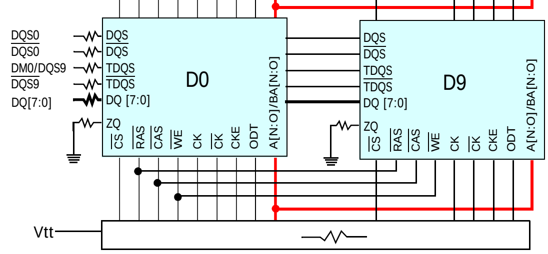
Note:
1.DQ-to-I/O wiring may be changed within byte.
2.ZQ resistors are 240Ω ±1%.For all other resistor values refer to the appropriate wiring diagram.

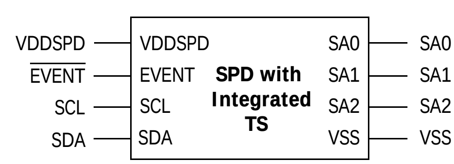


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

4GB, 512Mx72 Module(2Rank of x8) - page1

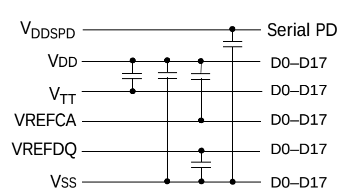




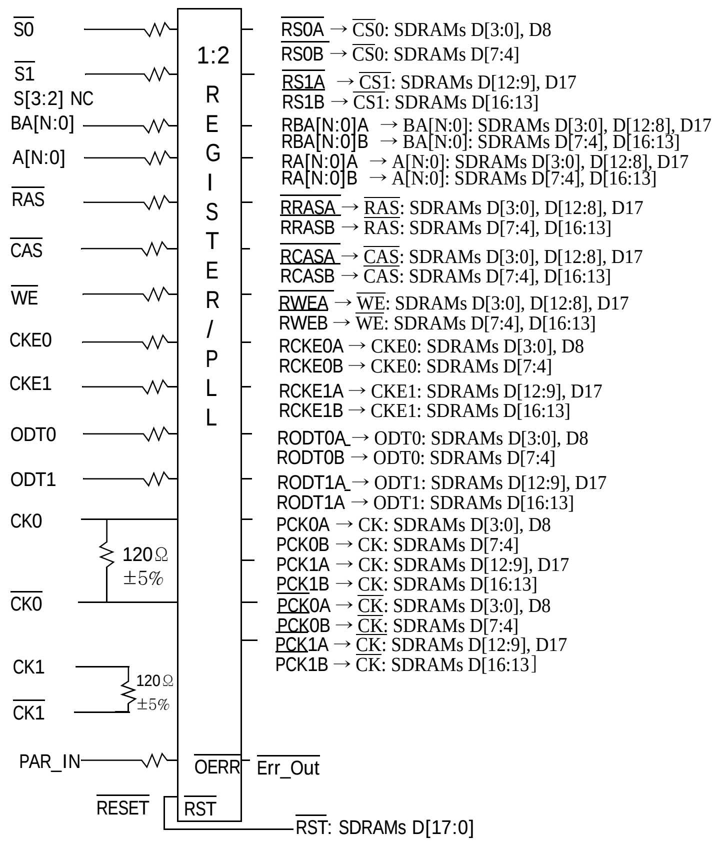


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

Note:
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 15Ω±5%.
3. ZQ resistors are 240Ω±1%. For all other resistor values refer to the appropriate wiring diagram.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.

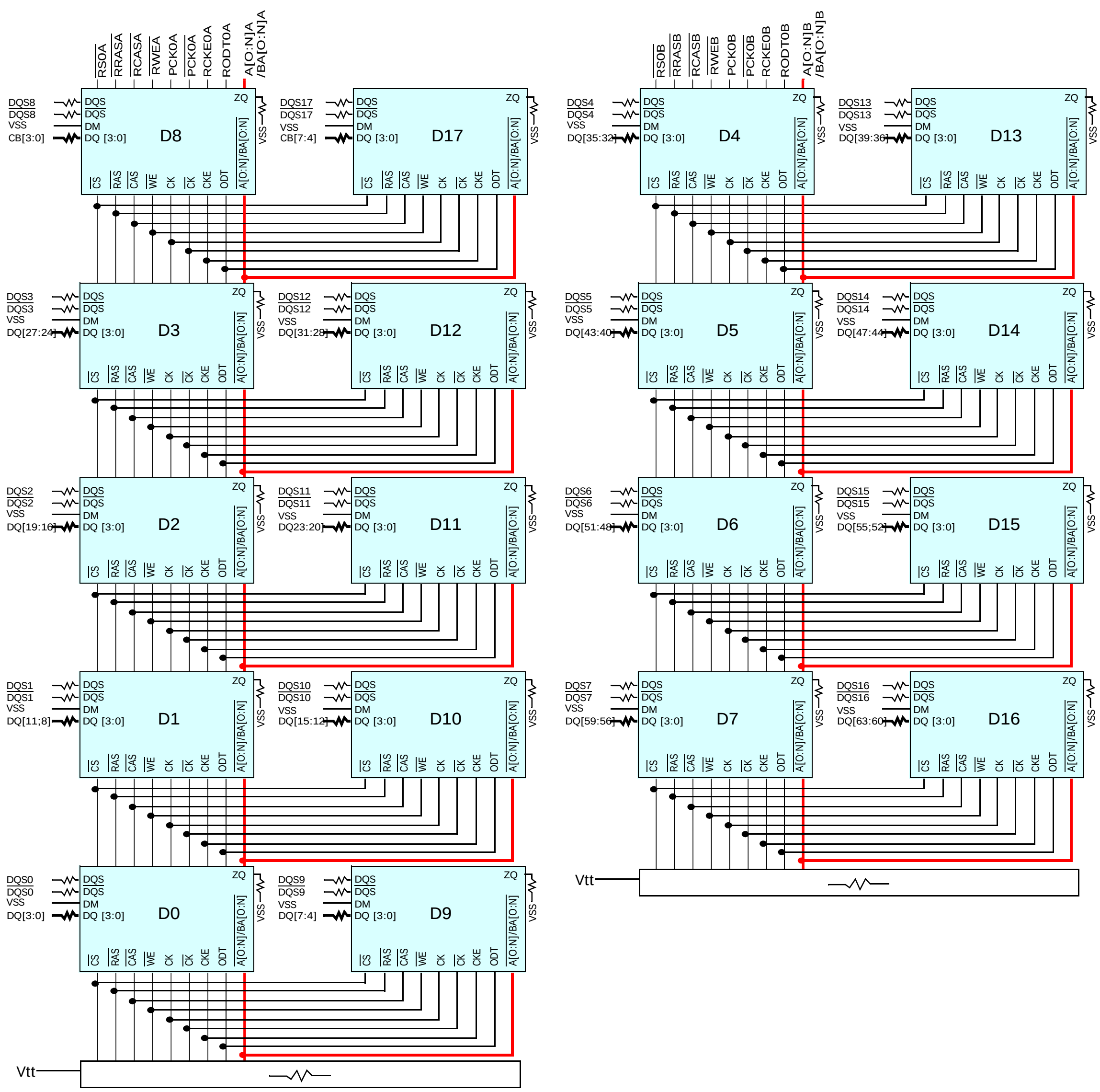


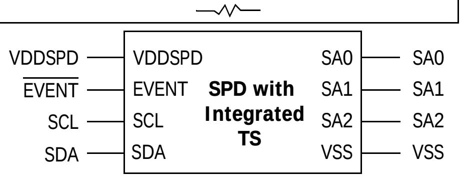
4GB, 512Mx72 Module(2Rank of x8) - page2



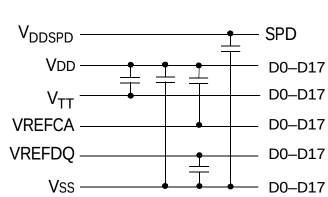
* S[3:2], CK1 and CK1 are NC

4GB, 512Mx72 Module(1Rank of x4) - page1



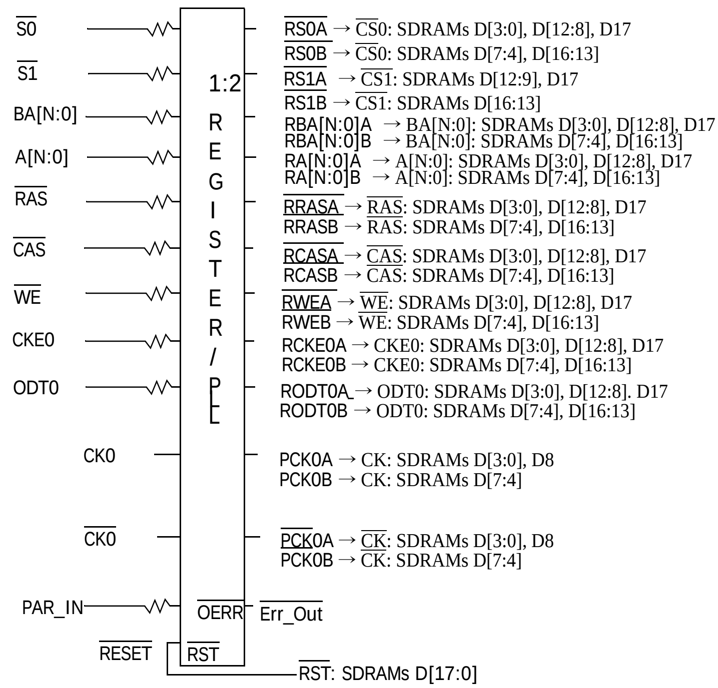


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative



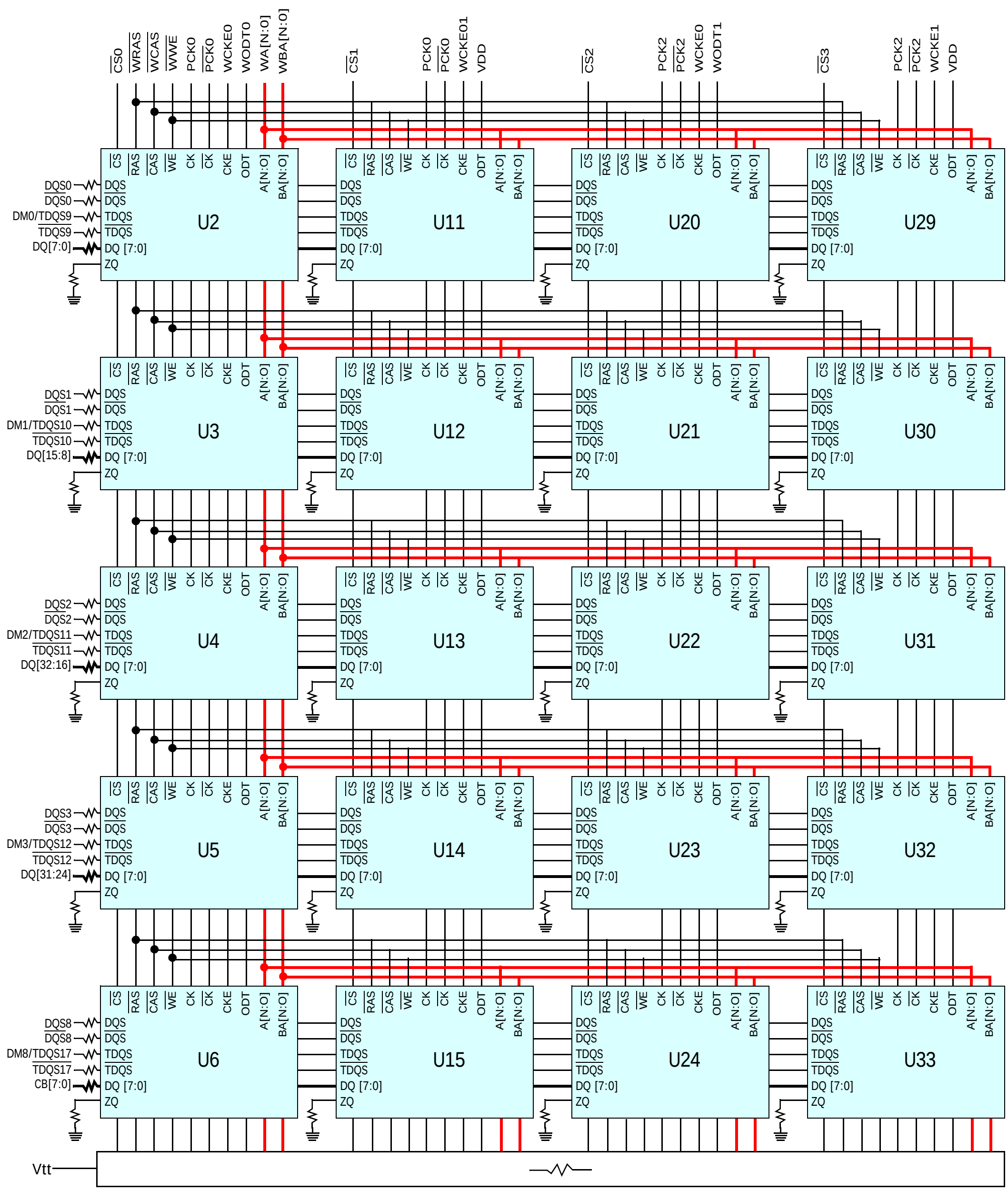
Note:
1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 15Ω ±5%.
3. See the wiring diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.

4GB, 512Mx72 Module(1Rank of x4) - page2

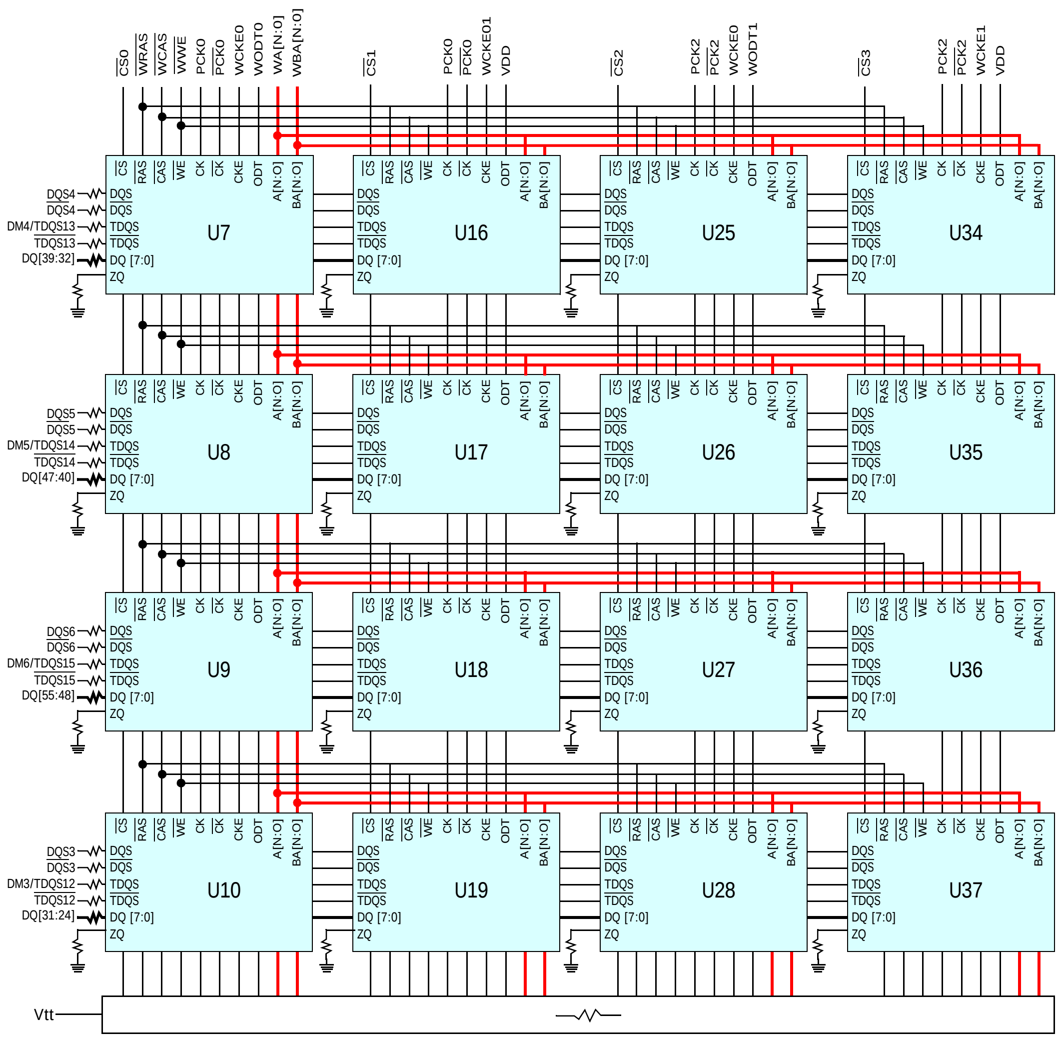


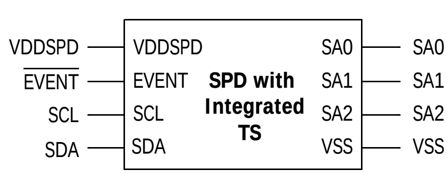
* S[3:2], CKE1, ODT1, CK1 and CK1 are NC (Unused register inputs ODT1 and CKE1 have a 330Ω resistor to ground.)

8GB, 1Gx72 Module(4Rank of x8) - page1

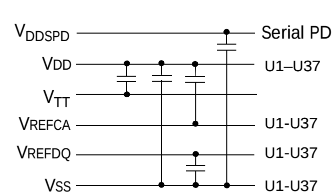


8GB, 1Gx72 Module(4Rank of x8) - page2



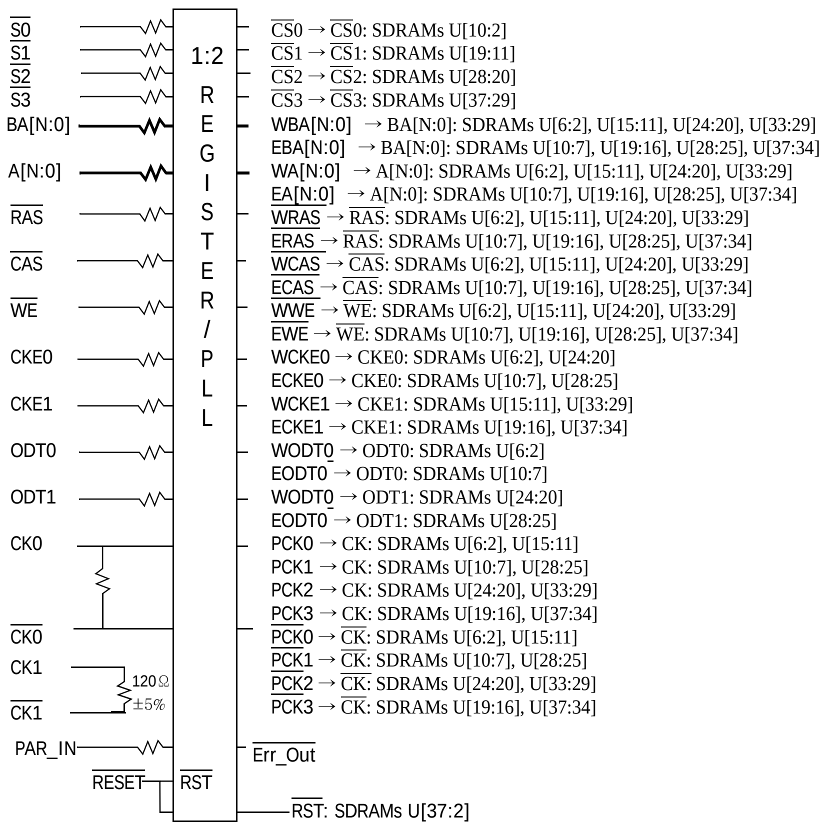


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative



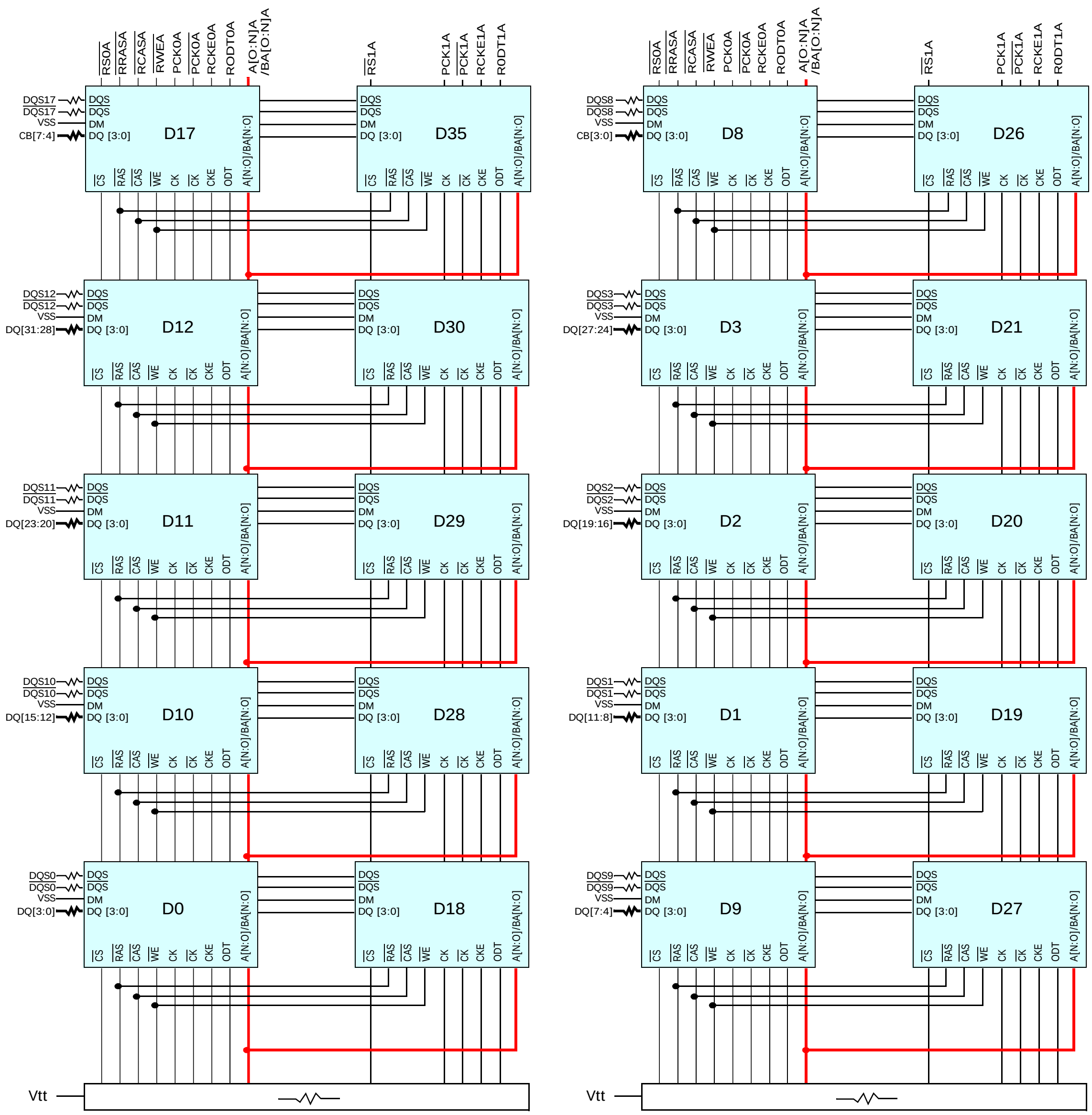
Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. See wiring diagrams for resistor values.
3. ZQ pins of each SDRAM are connected to individual RZQ resistors (240+/-1%) ohms.

8GB, 1Gx72 Module(4Rank of x8) - page3

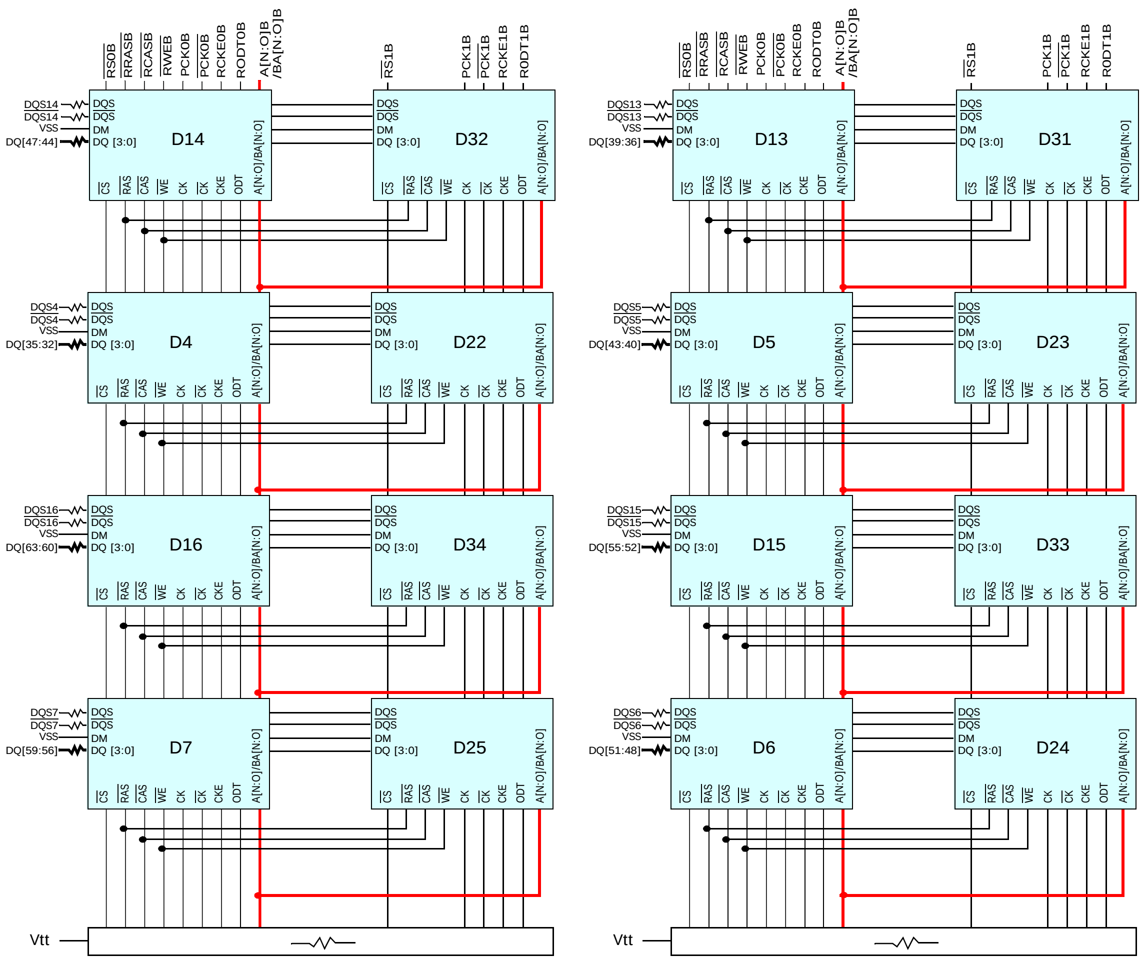


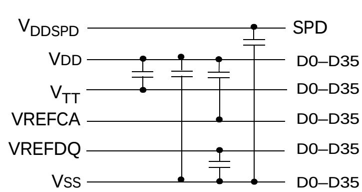
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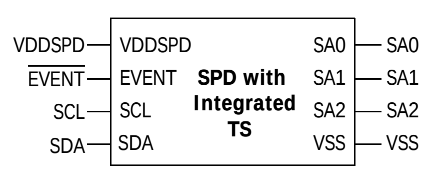
8GB, 1Gx72 Module(2Rank of x4) - page1



8GB, 1Gx72 Module(2Rank of x4) - page2





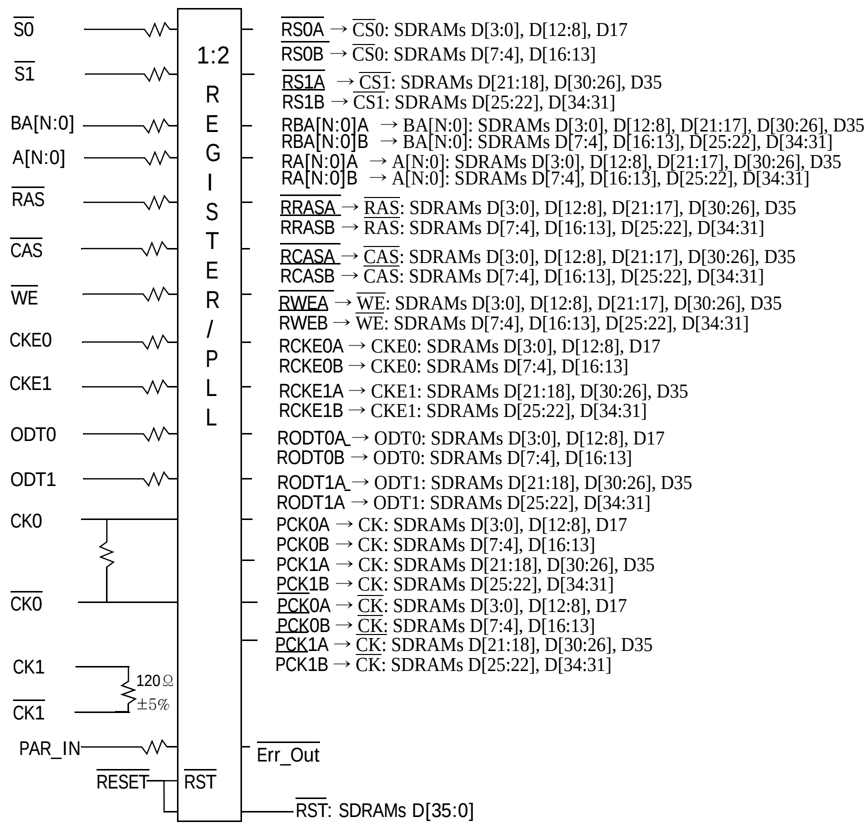


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

Note:

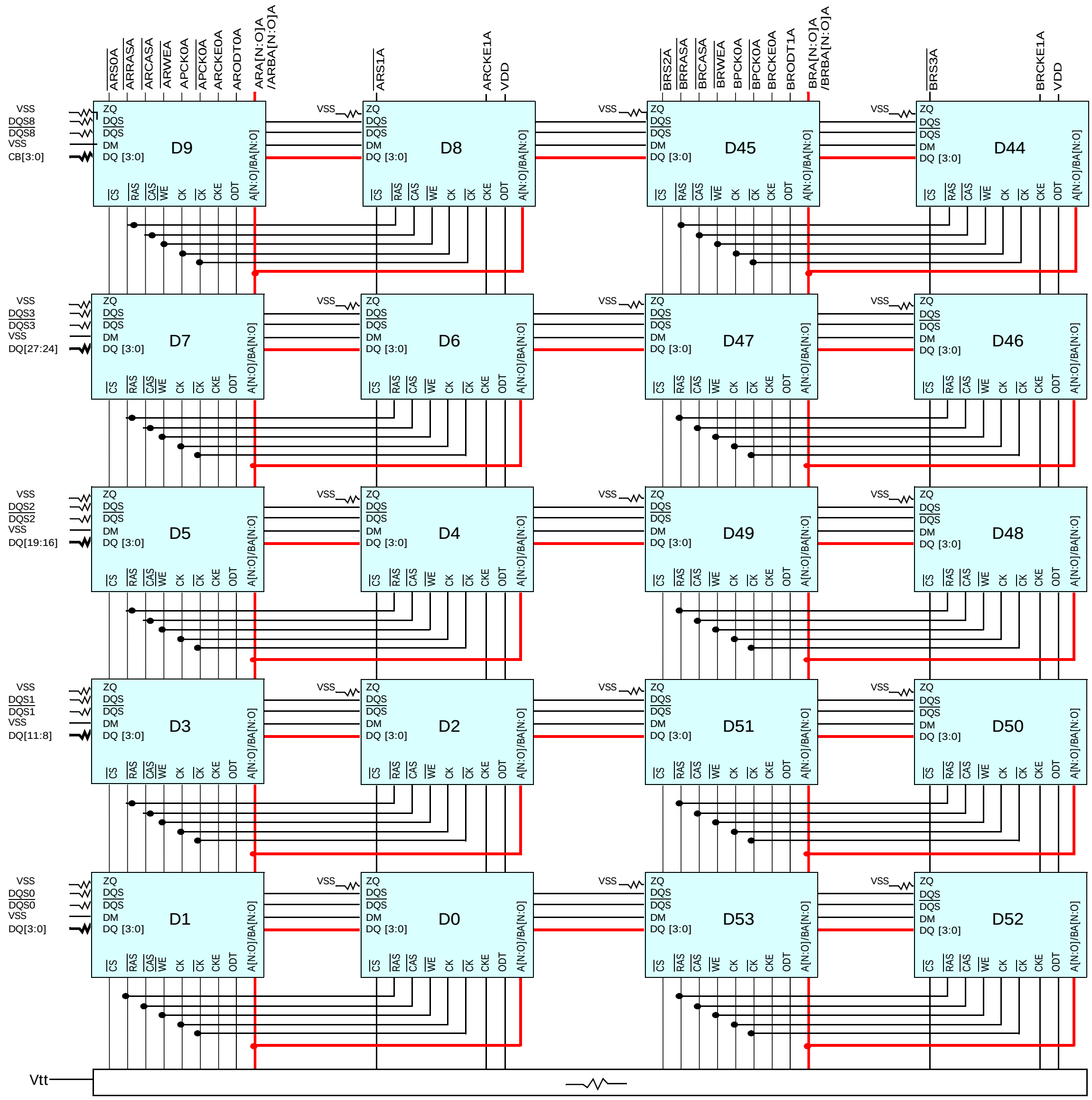
1. DQ-to-I/O wiring may be changed within a nibble.
2. See wiring diagrams for all resistors values.
3. ZQ pins of each SDRAM are connected to individual RZQ resistors (240+/-1%) ohms.

8GB, 1Gx72 Module(2Rank of x4) - page3



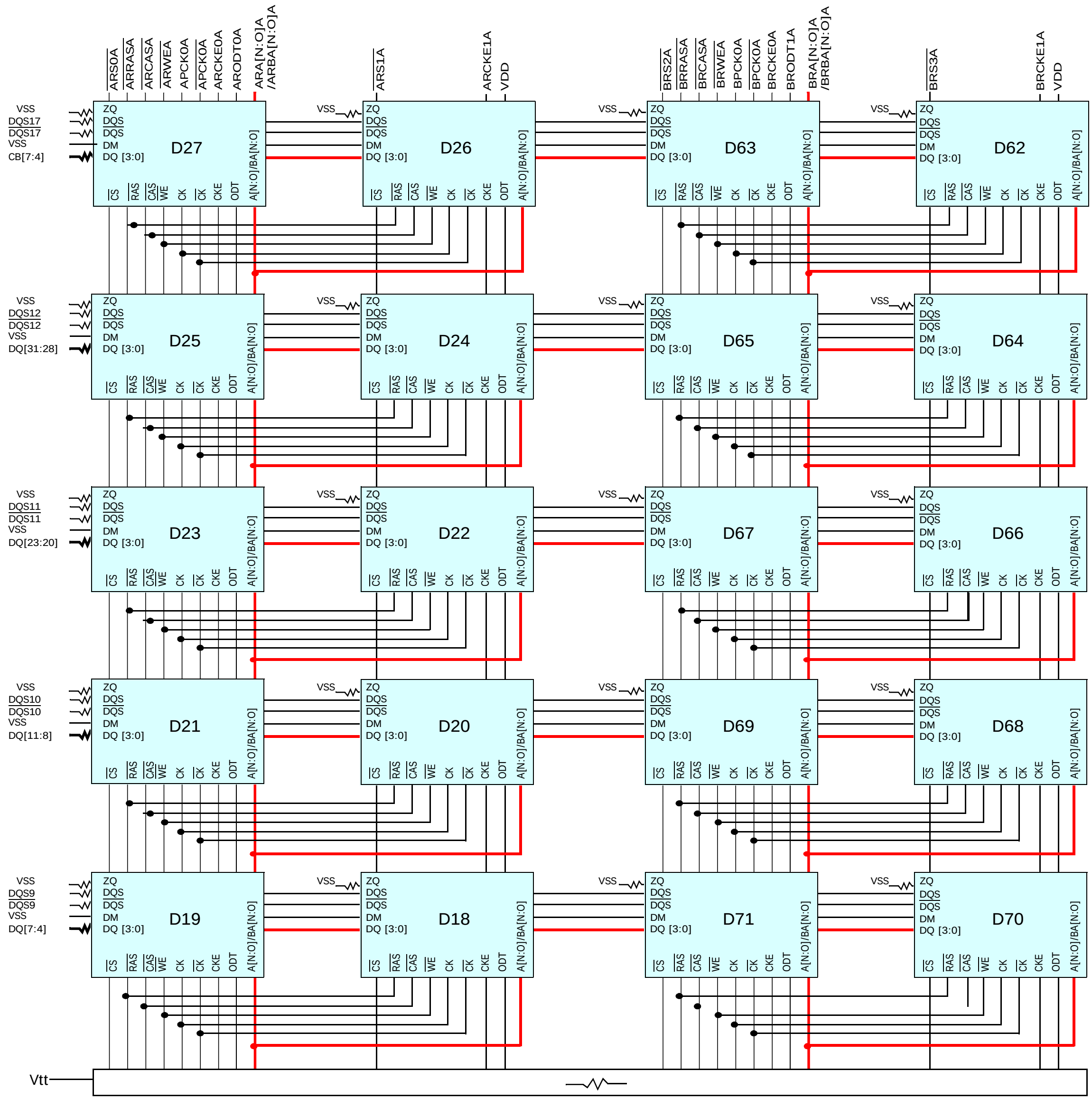
* S[3:2], CK1 and CK1 are NC

16GB, 2Gx72 Module(4Rank of x4) - page1

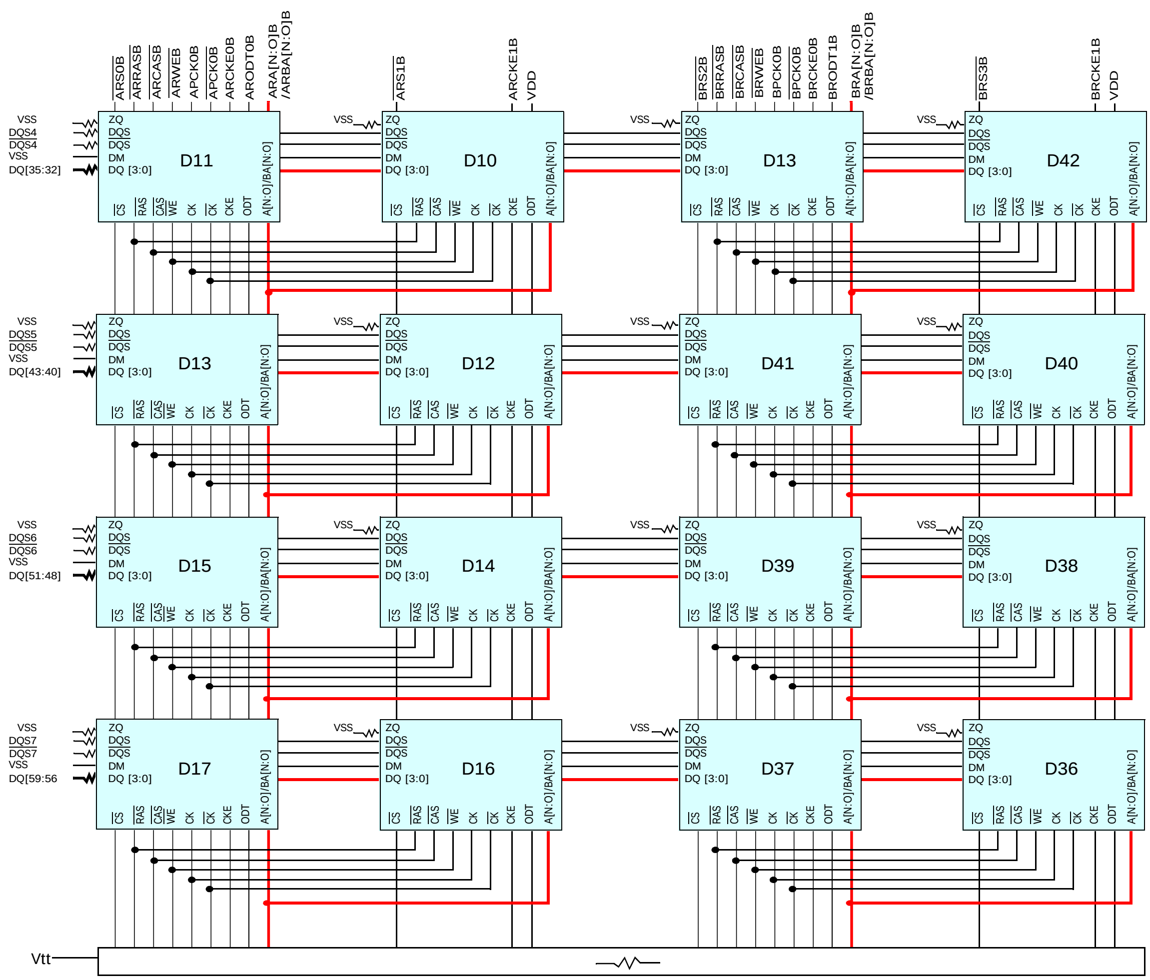


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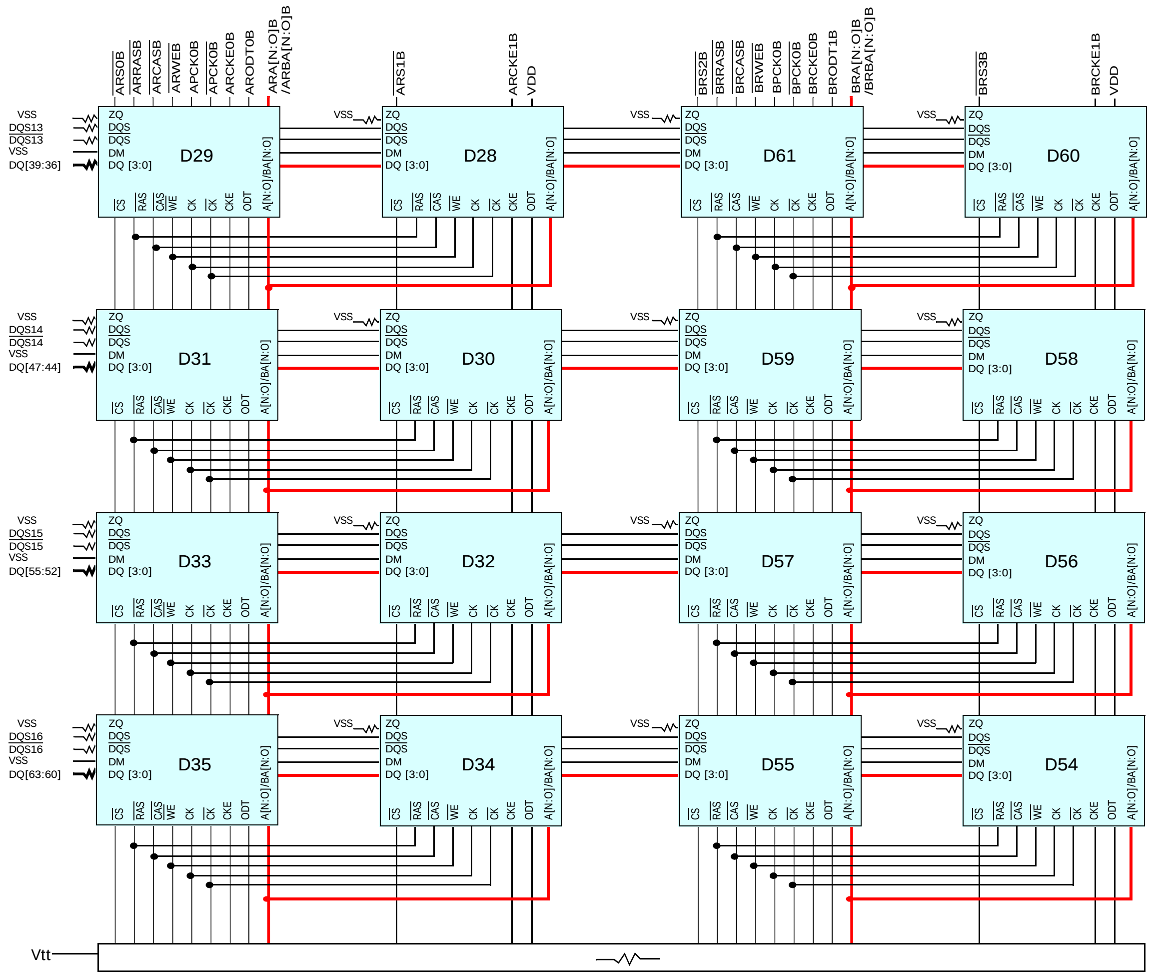
16GB, 2Gx72 Module(4Rank of x4) - page2

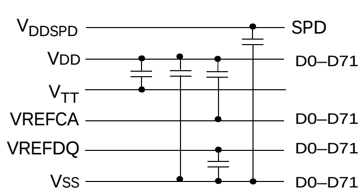


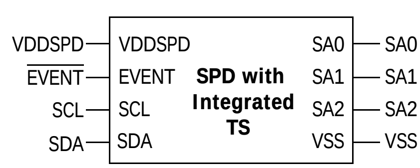
16GB, 2Gx72 Module(4Rank of x4) - page3



16GB, 2Gx72 Module(4Rank of x4) - page4





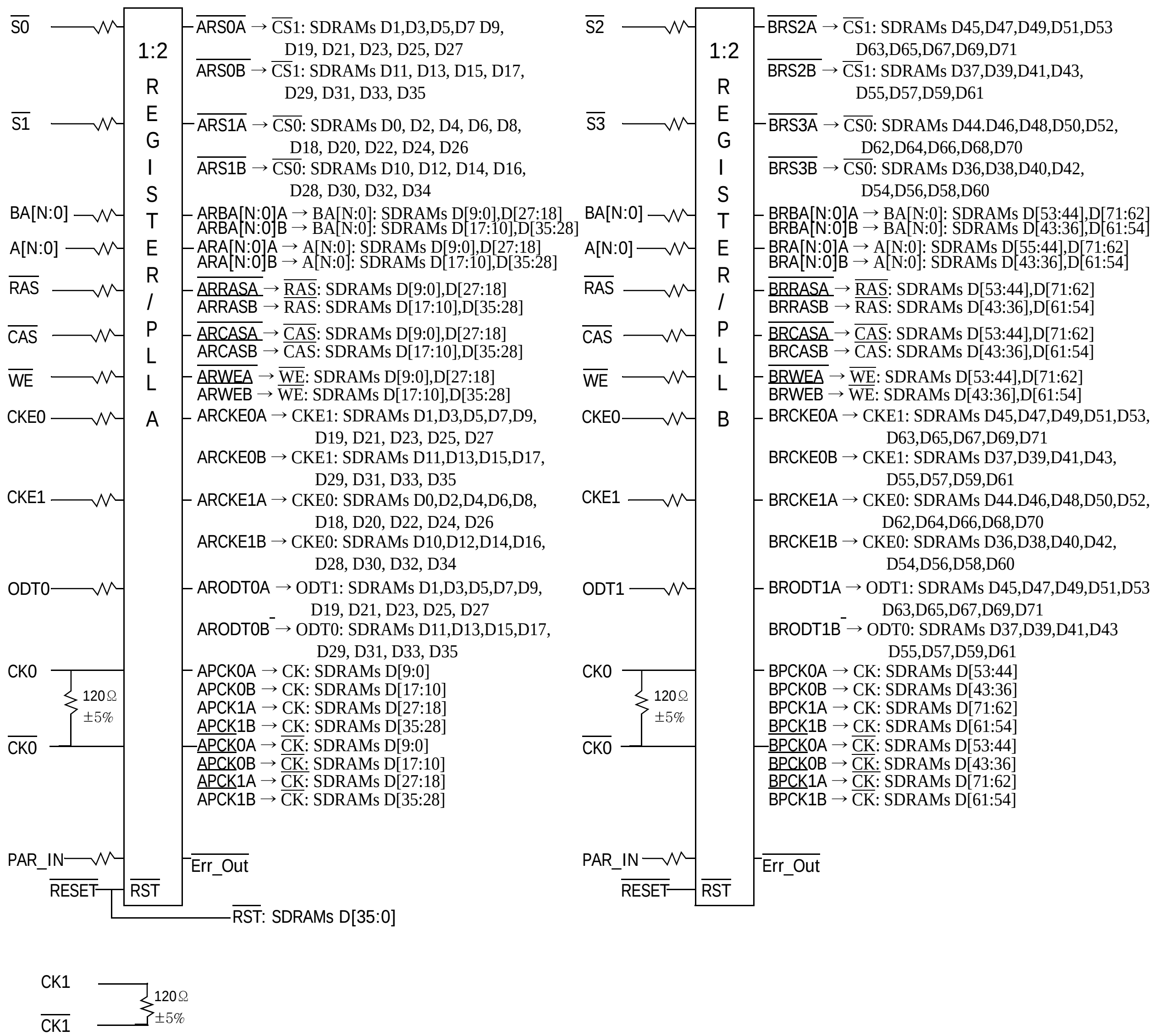


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

Note:

1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 15 Ohms ±5%.
3. See the wiring diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are 240 Ohms ±1%. For all other resistor values refer to the appropriate wiring diagram.

16GB, 2Gx72 Module(4Rank of x4) - page5



1. CK0 and CK0 are differentially terminated with a single 120 Ohms ±5% resistor.
2. CK1 and CK1 are differentially terminated with a single 120 Ohms ±5% resistor, but is not used.
3. Unused register inputs ODT1 for Register A and ODT0 for Register B are tied to ground.
4. The module drawing on this page is not drawn to scale.

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Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.80 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^oC	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^oC	1,2
	Extended Temperature Range	85 to 95	^oC	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR3 SDRAMs support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single Ended AC and DC Input Levels for Command and ADDress

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Notes
		Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1, 5
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1, 6
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2	V	1, 2, 7
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175	V	1, 2, 8
VIH.CA(AC150)	AC Input logic high	Vref + 0.150	Note2	V	1, 2, 7
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150	V	1, 2, 8
VIH.CA(AC135)	AC input logic high	-	-	V	1, 2, 7
VIL.CA(AC135)	AC input logic low	-	-	V	1, 2, 8
VIH.CA(AC125)	AC Input logic high	-	-	V	1, 2, 7
VIL.CA(AC125)	AC input logic low	-	-	V	1, 2, 8
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4, 9

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 43.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.CA(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.CA(DC100)
7. VIH(ac) is used as simplified symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135), and VIH.CA(AC125); VIH.CA(AC175) value is used when Vref + 0.175V is referenced, VIH.CA(AC150) value is used when Vref + 0.150V is referenced, VIH.CA(AC135) value is used when Vref + 0.135V is referenced, and VIH.CA(AC125) value is used when Vref + 0.125V is referenced.
8. VIL(ac) is used as simplified symbol for VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135), and VIL.CA(AC125); VIL.CA(AC175) value is used when Vref - 0.175V is referenced, VIL.CA(AC150) value is used when Vref - 0.150V is referenced, VIL.CA(AC135) value is used when Vref - 0.135V is referenced, and VIL.CA(AC125) value is used when Vref - 0.125V is referenced.
9. Vref is measured relative to VDD at the same point, time and same device.

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AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066 as specified in the table below. DDR3 SDRAM will also support corresponding tDS values (Table 41 and Table 47 in “ DDR3 Device Operation”) as well as derating tables in Table 44 of “DDR3 Device Operation” depending on Vih/Vil AC levels.

Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		Unit	Notes
		Min	Max	Min	Max		
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1, 5
VIL.DQ(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1, 6
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	Note2	-	-	V	1, 2, 7
VIL.DQ(AC175)	AC input logic low	Note2	Vref - 0.175	-	-	V	1, 2, 8
VIH.DQ(AC150)	AC Input logic high	Vref + 0.150	Note2	Vref + 0.150	Note2	V	1, 2, 7
VIL.DQ(AC150)	AC input logic low	Note2	Vref - 0.150	Note2	Vref - 0.150	V	1, 2, 8
VIH.CA(AC135)	AC input logic high	-	-	-	-	mV	1, 2, 7
VIL.CA(AC135)	AC input logic low	-	-	-	-	mV	1, 2, 8
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4, 9

Notes:

1. Vref = VrefDQ (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 43.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. VIH(dc) is used as a simplified symbol for VIH.DQ(DC100)
6. VIL(dc) is used as a simplified symbol for VIL.DQ(DC100)
7. VIH(ac) is used as simplified symbol for VIH.DQ(AC175), VIH.DQ(AC150), and VIH.DQ(AC135); VIH.DQ(AC175) value is used when Vref + 0.175V is referenced, VIH.DQ(AC150) value is used when Vref + 0.150V is referenced, and VIH.DQ(AC135) value is used when Vref + 0.135V is referenced.
8. VIL(ac) is used as simplified symbol for VIL.DQ(AC175), VIL.DQ(AC150), and VIL.DQ(AC135); VIL.DQ(AC175) value is used when Vref - 0.175V is referenced, VIL.DQ(AC150) value is used when Vref - 0.150V is referenced, and VIL.DQ(AC135) value is used when Vref - 0.135V is referenced.
9. Vref is measured relative to VDD at the same point, time and same device.

Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages $_{VRefCA}$ and V_{RefDQ} are illustrated in figure below. It shows a valid reference voltage V_{Ref} (t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

V_{Ref} (DC) is the linear average of V_{Ref} (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table "Differential Input Slew Rate Definition" on page 38. Furthermore V_{Ref} (t) may temporarily deviate from $V_{Ref\ (DC)}$ by no more than +/- 1% VDD.

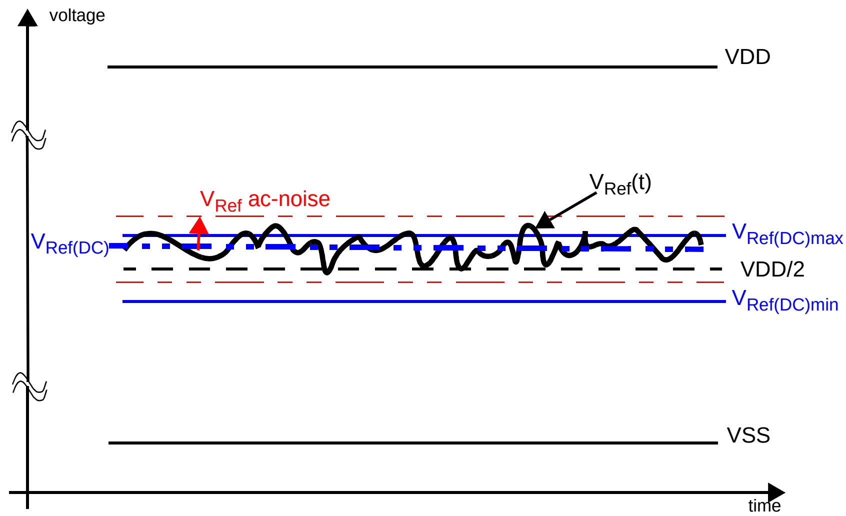


Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

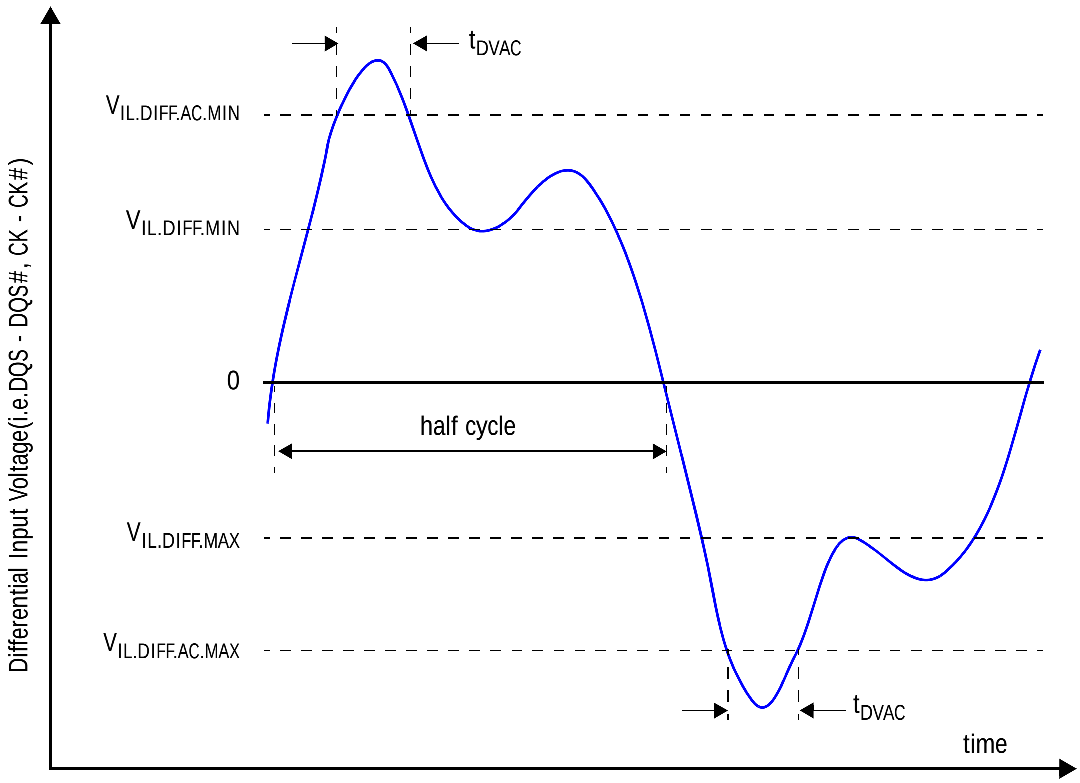
"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in figure above.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref}ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK - $\overline{\text{CK}}$) and strobe (DQS-$\overline{\text{DQS}}$)

Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800, 1066, 1333, 1600		Unit	Notes
		Min	Max		
VIHdiff	Differential input high	+ 0.200	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.200	V	1
VIHdiff (ac)	Differential input high ac	2 x (VIH (ac) - Vref)	Note 3	V	2
VILdiff (ac)	Differential input low ac	Note 3	2 x (VIL (ac) - Vref)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - $\overline{\text{CK}}$ use VIH/VIL (ac) of AADD/CMD and VREFCA; for DQS - $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ use VIH/VIL (ac) of DQs and VREFDQ; if a reduced ac-high or ac-low levels is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 43.

Allowed time before ringback (tDVAC) for CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff (ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

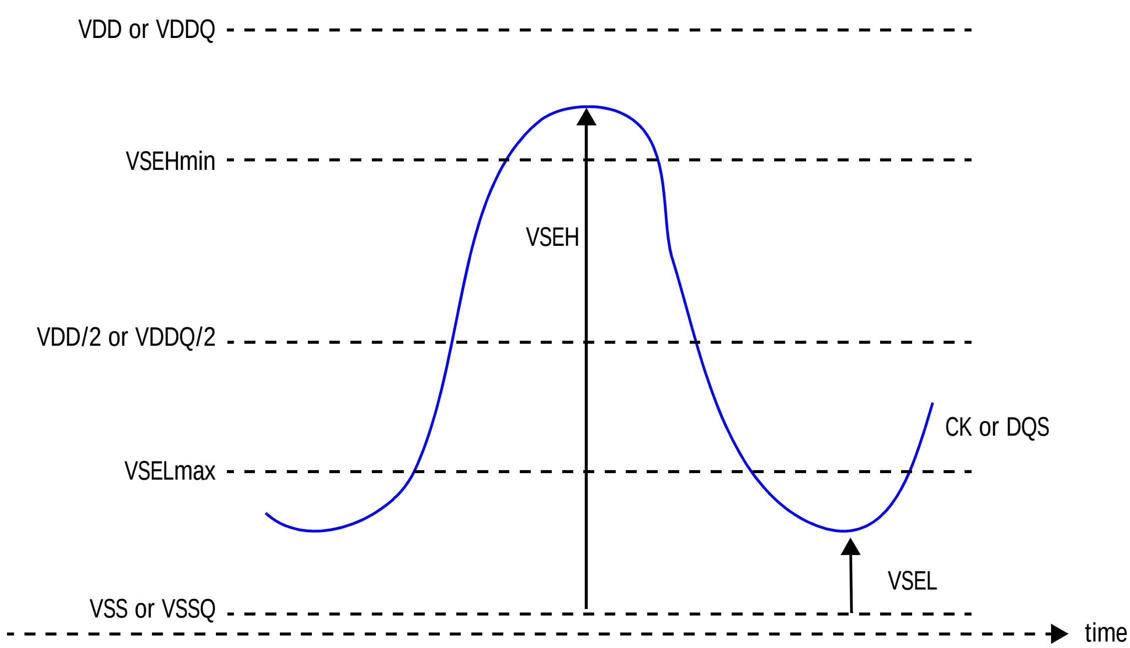
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, of $\overline{\text{DQSU}}$) has also to comply with certain requirements for single-ended signals.

CK and CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{\text{CK}}$.



Single-ended requirements for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. the transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

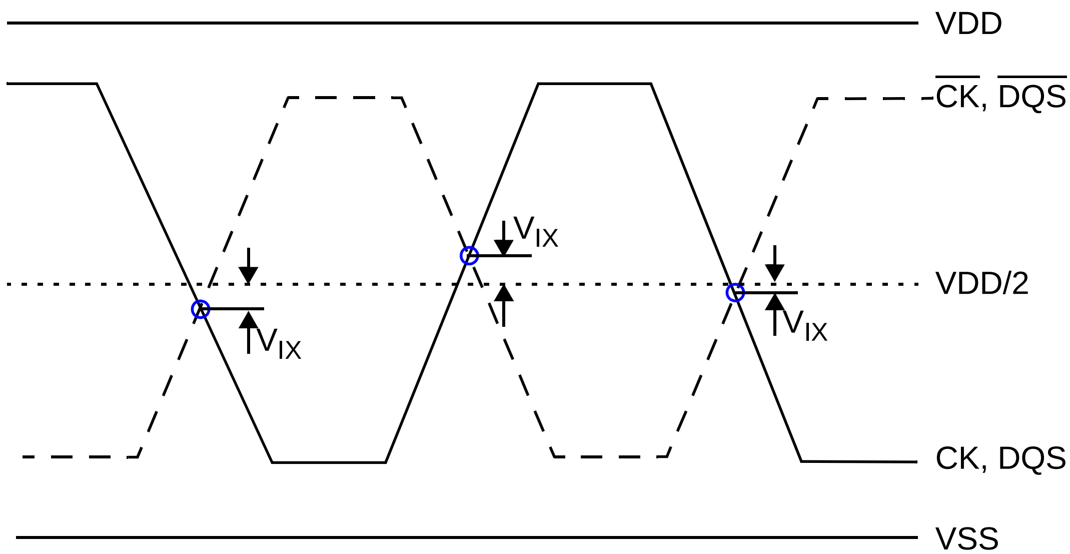
Symbol	Parameter	DDR3-800, 1066, 1333, 1600		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for Ck, $\overline{CK}$	(VDD /2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) = 0.175	V	1,2
	Single-ended low level for CK, $\overline{CK}$	Note 3	(VDD / 2) = 0.175	V	1,2

Notes:

1. For CK, $\overline{CK}$ use VIH/VIL (ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL (ac) of DQs.
2. VIH (ac)/VIL (ac) for DQs is based on VREFDQ; VIH (ac)/VIL (ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 43.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, 1066, 1333, 1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.
2. Refer to the table "Single-ended levels for CK, DQS, DQSL, DQSU, CK, DQS, DQSL or DQSU" on page 36 for VSEL and VSEH standard values.

Slew Rate Definitions for Single-Ended Input Signals

See 7.5 “Address / Command Setup, Hold and Derating” on page 137 in “DDR3 Device Operation” for single-ended slew rate definitions for address and command signals.

See 7.6 “Data Setup, Hold and Slew Rate Derating” on page 144 in “DDR3 Device Operation” for single-ended slew rate definition for data signals.

Slew Rate Definitions for Differential Input Signals

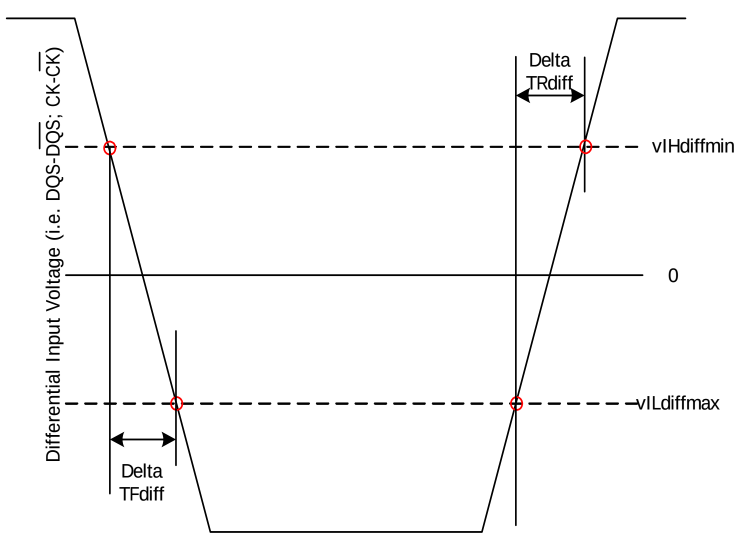
Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in table and figure below.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff

Notes:

The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

AC & DC Output Measurement Levels

Single Ended AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes:

1. The swing of ±0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ} / 2.

Differential AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
$V_{OHdiff\ (AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff\ (AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Notes:

1. The swing of ±0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

Single Ended Output Slew Rate

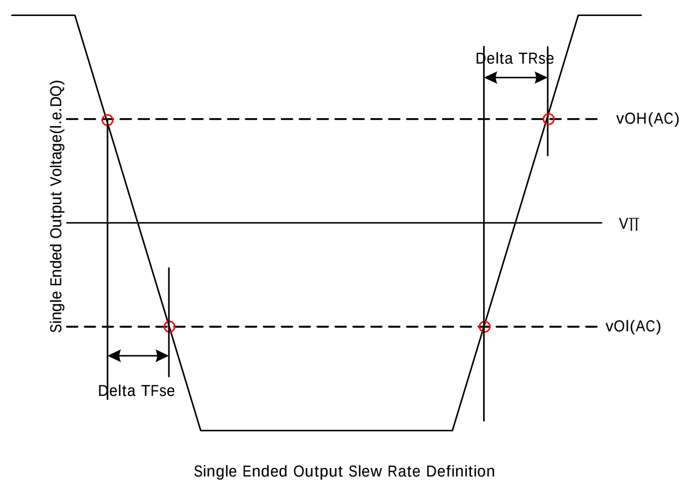
When the Reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals are shown in table and figure below.

Single-ended Output slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)}-V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)}-V_{OL(AC)}]$ / DeltaTFse

Notes:

1. Output slew rate is verified by design and characterisation, and may not be subject to production test.



Single Ended Output slew Rate Definition

Output Slew Rate (single-ended)

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note 1): In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

Case 1 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

Case 2 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane switching into the opposite direction (i.e. from low to high of high to low respectively). For the remaining DQ signal switching in to the opposite direction, the regular maximum limite of 5 V/ns applies.

Differential Output Slew Rate

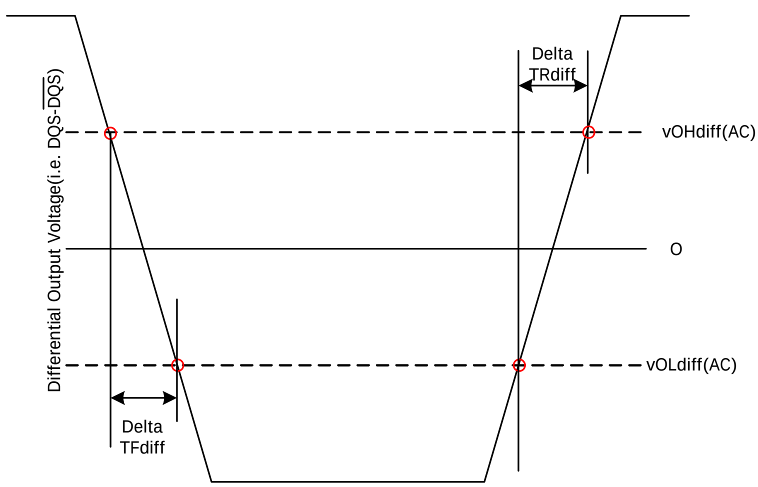
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in table and figure below.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff\ (AC)}$	$V_{OHdiff\ (AC)}$	[$V_{OHdiff\ (AC)}$-$V_{OLdiff\ (AC)}$] / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff\ (AC)}$	$V_{OLdiff\ (AC)}$	[$V_{OHdiff\ (AC)}$-$V_{OLdiff\ (AC)}$] / DeltaTFdiff

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential Output slew Rate Definition

Differential Output Slew Rate

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	12	5	12	5	12	5	12	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

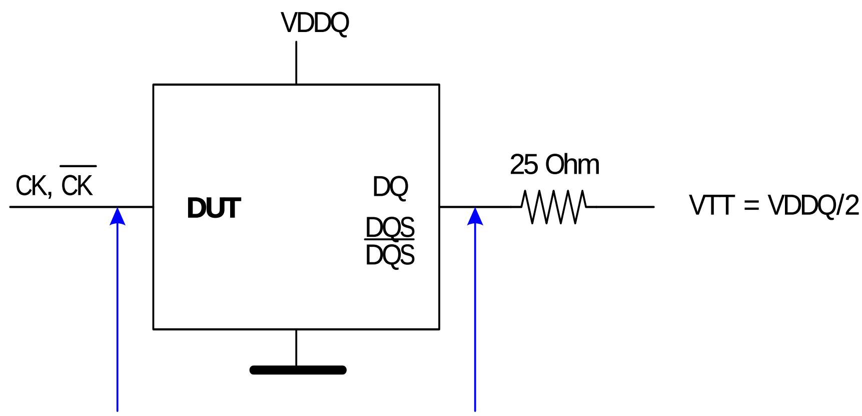
se: Single-ended Signals

For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

Figure below represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

Overshoot and Undershoot Specifications

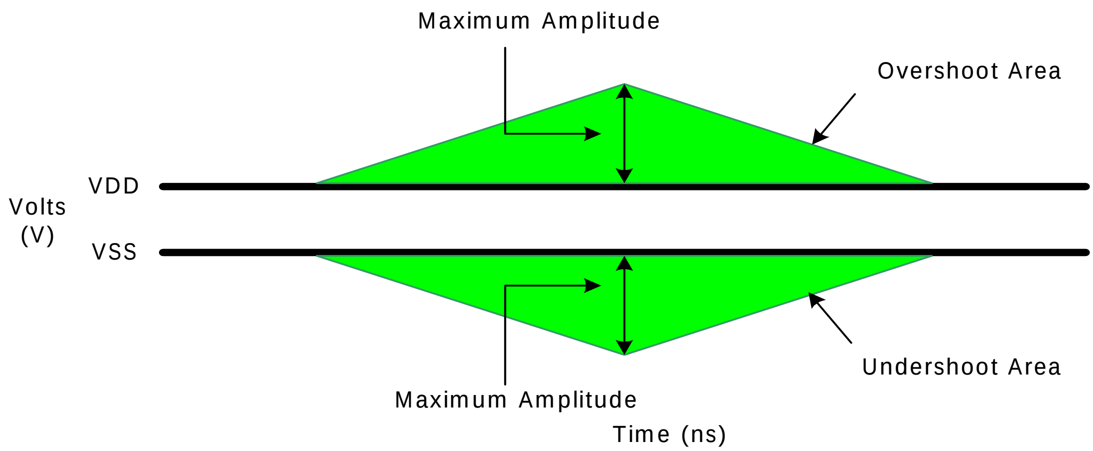
Address and Control Overshoot and Undershoot Specifications

AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area. (See figure below)	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See figure below)	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See figure below)	0.67	0.5	0.4	0.33	V-ns
Maximum undershoot area below VSS (See figure below)	0.67	0.5	0.4	0.33	V-ns

(A0-A15, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT)

See figure below for each parameter definition



Address and Control Overshoot and Undershoot Definition

Address and Control Overshoot and Undershoot Definition

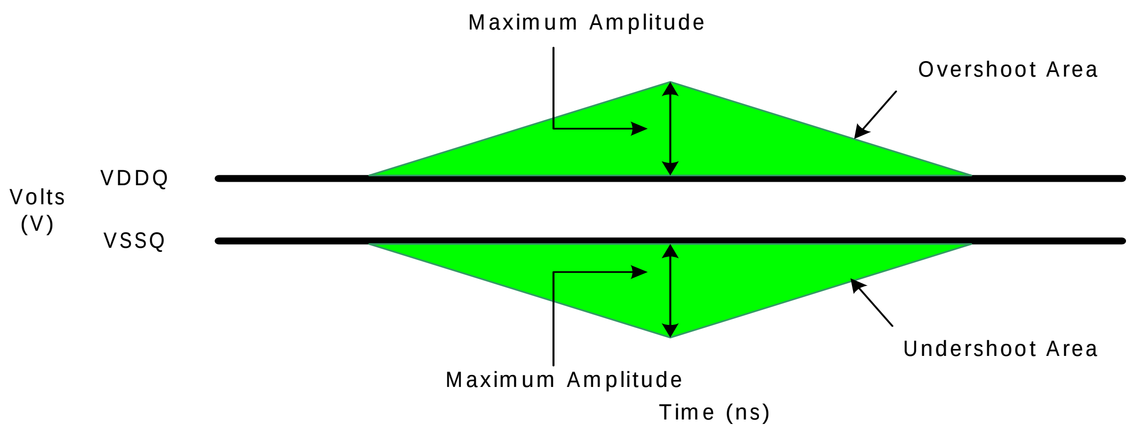
Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area (See figure below)	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area (See figure below)	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See figure below)	0.25	0.19	0.15	0.13	V-ns
Maximum undershoot area below VSS (See figure below)	0.25	0.19	0.15	0.13	V-ns

(CK, $\overline{\text{CK}}$, DQ, DQS, $\overline{\text{DQS}}$, DM)

See figure below for each parameter definition



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

Refresh parameters by device density

Refresh parameters by device density

Parameter	RTT_Nom Setting		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command ACT or REF command time	tRFC		90	110	160	260	350	ns	
Average periodic refresh interval	tREFI	$0\ °C \le T_{CASE} \le 85\ °C$	7.8	7.8	7.8	7.8	7.8	us	
		$85\ °C < T_{CASE} \le 95\ °C$	3.9	3.9	3.9	3.9	3.9	us	1

Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-800 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50.

Speed Bin			DDR3-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3
Supported CL Settings			6		n_{CK}	
Supported CWL Settings			5		n_{CK}	

DDR3-1066 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50.

Speed Bin		DDR3-1066F		Unit	Note
CL - nRCD - nRP		7-7-7			
Parameter	Symbol	min	max		
Internal read command to first data	t_{AA}	13.125	20	ns	
ACT to internal read or write delay time	t_{RCD}	13.125	—	ns	
PRE command period	t_{RP}	13.125	—	ns	
ACT to ACT or REF command period	t_{RC}	50.625	—	ns	
ACT to PRE command period	t_{RAS}	37.5	9 * tREFI	ns	
CL = 6, CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,6
CL = 6, CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 7, CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7, CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4
CL = 8, CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8, CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3
Supported CL Settings		6, 7, 8		n_{CK}	
Supported CWL Settings		5, 6		n_{CK}	

DDR3-1333 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50.

Speed Bin			DDR3-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5 (13.125)[5,10]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5 (13.125)[5,10]	—	ns	
PRE command period		t_{RP}	13.5 (13.125)[5,10]	—	ns	
ACT to ACT or REF command period		t_{RC}	49.5 (49.125)[5,10]	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)[5,10]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6, 7, 8, 9, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

DDR3-1600 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 50.

Speed Bin			DDR3-1600K		Unit	Note
CL - nRCD - nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.75 (13.125)[5,10]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.75 (13.125)[5,10]	—	ns	
PRE command period		t_{RP}	13.75 (13.125)[5,10]	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75 (48.125)[5,10]	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,8
			(Optional)[5,10]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4,8
			(Optional)[5,10]			
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to Hynix DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	^oC	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

IDD and IDDQ Specification Parameters and Test Conditions

IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}

Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

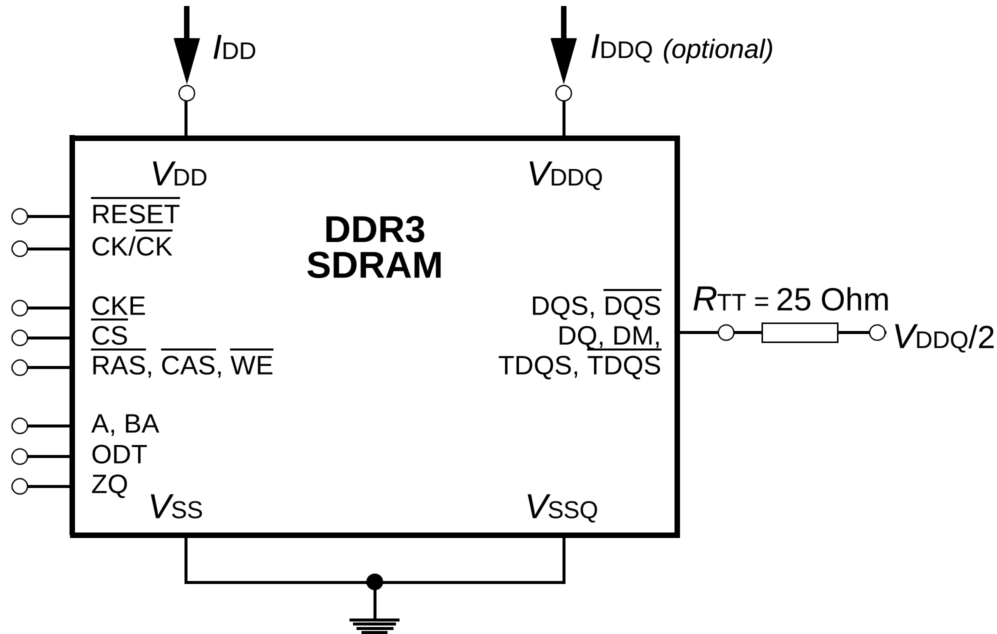


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above

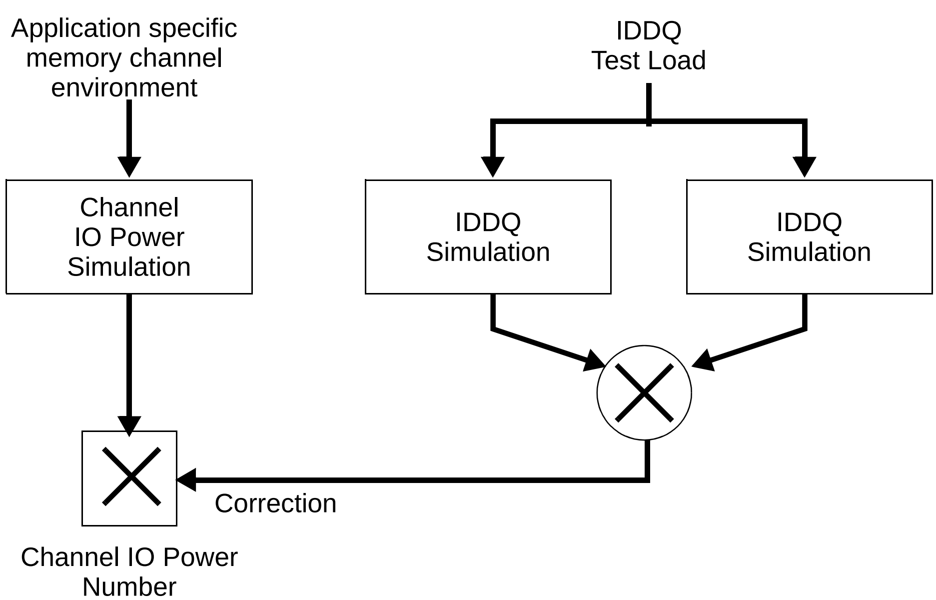


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-1066	DDR3-1333	DDR3-1600	Unit
		7-7-7	9-9-9	11-11-11	
t_{CK}		1.875	1.5	1.25	ns
CL		7	9	11	nCK
n_{RCD}		7	9	11	nCK
n_{RC}		27	33	39	nCK
n_{RAS}		20	24	28	nCK
n_{RP}		7	9	11	nCK
n_{FAW}	1KB page size	20	20	24	nCK
	2KB page size	27	30	32	nCK
n_{RRD}	1KB page size	4	4	5	nCK
	2KB page size	6	5	6	nCK
n_{RFC} -512Mb		48	60	72	nCK
n_{RFC}-1 Gb		59	74	88	nCK
n_{RFC}- 2 Gb		86	107	128	nCK
n_{RFC}- 4 Gb		139	174	208	nCK
n_{RFC}- 8 Gb		187	234	280	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3.
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4.

Symbol	Description
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c)]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c)]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 ^{o}C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Normal[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range (optional) T_{CASE}: 0 - 95 ^{o}C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Extended[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL

Symbol	Description
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a),f)]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID_LEVEL.

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Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

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Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}$, $\overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications (Tcase: 0 to 95°C)

* Module IDD values in the datasheet are only a calculation based on the component IDD spec.
The actual measurements may vary according to DQ loading cap.

2GB, 256M x 72 R-DIMM: HMT325R7BFR8C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	1169	1214	1259	mA	
IDD1	1259	1304	1349	mA	
IDD2N	689	1034	1034	mA	
IDD2NT	1052	1079	1124	mA	
IDD2P0	336	336	336	mA	
IDD2P1	363	363	363	mA	
IDD2Q	989	1034	1034	mA	
IDD3N	1034	1079	1124	mA	
IDD3P	363	363	363	mA	
IDD4R	1484	1619	1709	mA	
IDD4W	1484	1619	1754	mA	
IDD5B	2114	2159	2294	mA	
IDD6	336	336	336	mA	
IDD6ET	363	363	363	mA	
IDD7	2159	2474	2519	mA	

4GB, 512M x 72 R-DIMM: HMT351R7BFR8C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	1394	1484	1619	mA	
IDD1	1484	1574	1709	mA	
IDD2N	1214	1304	1304	mA	
IDD2NT	1340	1394	1484	mA	
IDD2P0	444	444	444	mA	
IDD2P1	498	498	498	mA	
IDD2Q	1214	1304	1304	mA	
IDD3N	1304	1394	1484	mA	
IDD3P	498	498	498	mA	
IDD4R	1709	1889	2069	mA	
IDD4W	1709	1889	2114	mA	
IDD5B	2339	2429	2654	mA	
IDD6	444	444	444	mA	
IDD6ET	498	498	498	mA	
IDD7	2339	2699	2834	mA	

4GB, 512M x 72 R-DIMM: HMT351R7BFR4C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	1574	1664	1754	mA	
IDD1	1754	1844	1934	mA	
IDD2N	1214	1304	1304	mA	
IDD2NT	1340	1394	1484	mA	
IDD2P0	444	444	444	mA	
IDD2P1	498	498	498	mA	
IDD2Q	1214	1304	1304	mA	
IDD3N	1304	1394	1484	mA	
IDD3P	498	498	498	mA	
IDD4R	2204	2474	2654	mA	
IDD4W	2204	2474	2744	mA	
IDD5B	3464	3554	3824	mA	
IDD6	444	444	444	mA	
IDD6ET	498	498	498	mA	
IDD7	3554	4184	4274	mA	

8GB, 1G x 72 R-DIMM: HMT31GR7BFR8C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	1844	2024	2339	mA	
IDD1	1934	2114	2429	mA	
IDD2N	1664	1844	1844	mA	
IDD2NT	1916	2024	2204	mA	
IDD2P0	660	660	660	mA	
IDD2P1	768	768	768	mA	
IDD2Q	1664	1844	1844	mA	
IDD3N	1844	2024	2204	mA	
IDD3P	768	768	768	mA	
IDD4R	2159	2429	2789	mA	
IDD4W	2159	2429	2834	mA	
IDD5B	2789	2969	3374	mA	
IDD6	660	660	660	mA	
IDD6ET	768	768	768	mA	
IDD7	2699	3149	3464	mA	

8GB, 1G x 72 R-DIMM: HMT31GR7BFR4C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	2024	2204	2474	mA	
IDD1	2204	2384	2654	mA	
IDD2N	1664	1844	1844	mA	
IDD2NT	1916	2024	2204	mA	
IDD2P0	660	660	660	mA	
IDD2P1	768	768	768	mA	
IDD2Q	1664	1844	1844	mA	
IDD3N	1844	2024	2204	mA	
IDD3P	768	768	768	mA	
IDD4R	2654	3014	3374	mA	
IDD4W	2654	3014	3464	mA	
IDD5B	3914	4094	4544	mA	
IDD6	660	660	660	mA	
IDD6ET	768	768	768	mA	
IDD7	3914	4634	4904	mA	

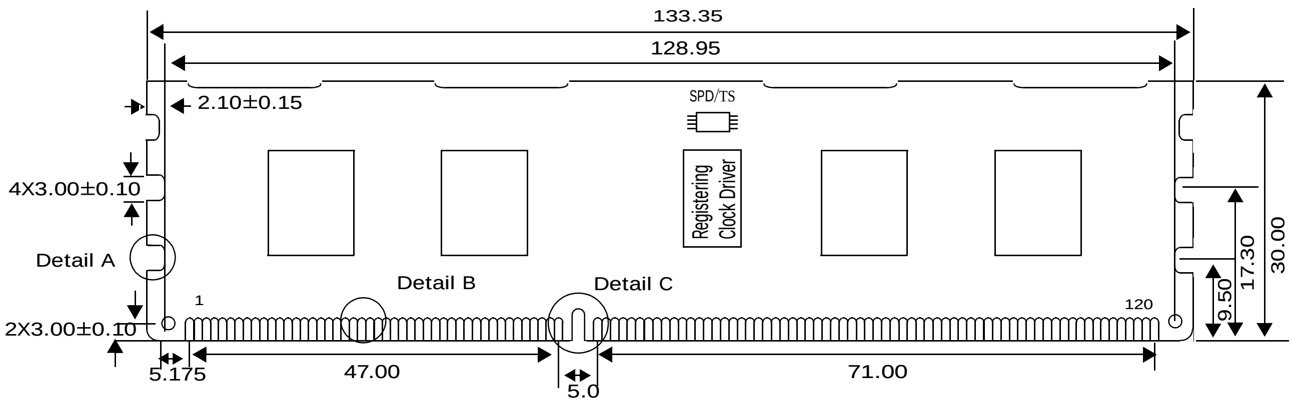
16GB, 2G x 72 R-DIMM: HMT42GR7BMR4C

Symbol	DDR3 1066	DDR3 1333	DDR3 1600	Unit	note
IDD0	2924	3284	3914	mA	
IDD1	3104	3464	4094	mA	
IDD2N	2564	2924	2924	mA	
IDD2NT	3068	3284	3644	mA	
IDD2P0	1092	1092	1092	mA	
IDD2P1	1308	1308	1308	mA	
IDD2Q	2564	2924	2924	mA	
IDD3N	2924	3284	3644	mA	
IDD3P	1308	1308	1308	mA	
IDD4R	3554	4094	4814	mA	
IDD4W	3554	4094	4904	mA	
IDD5B	4814	5174	5984	mA	
IDD6	1092	1092	1092	mA	
IDD6ET	1308	1308	1308	mA	
IDD7	4634	5534	6164	mA	

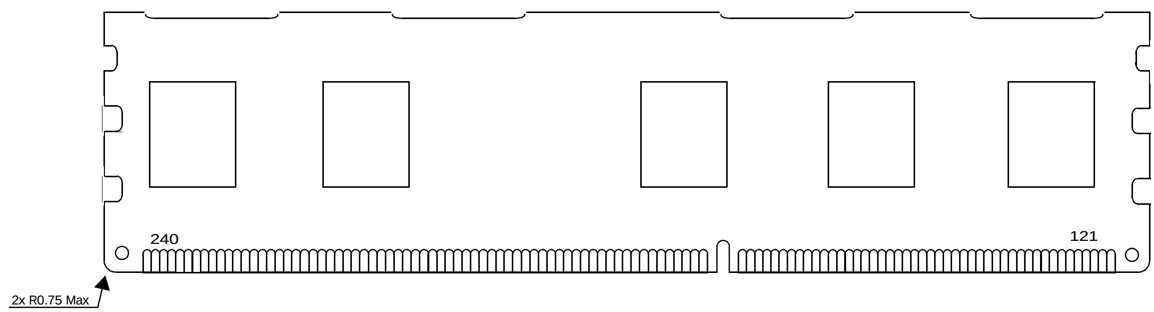
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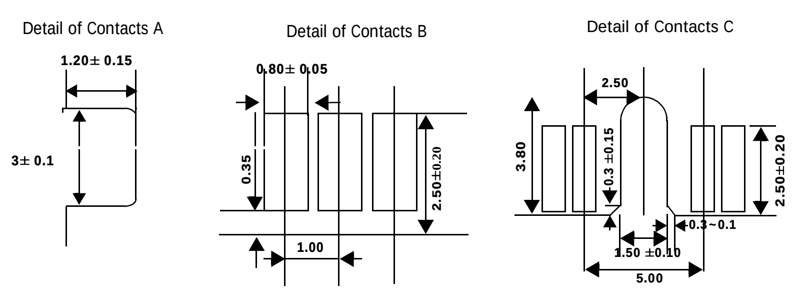
256Mx72 - HMT325R7BFR8C

Front

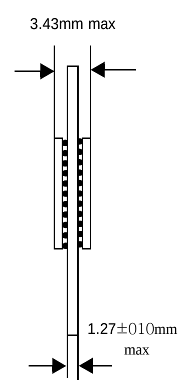


Back





Side

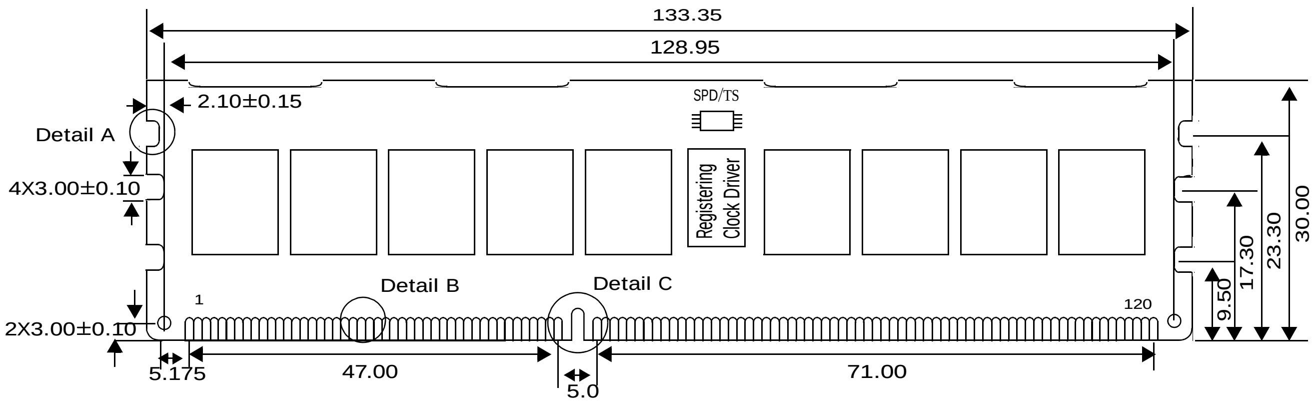


Note:
1. ±0.13 tolerance on all dimensions unless otherwise stated.

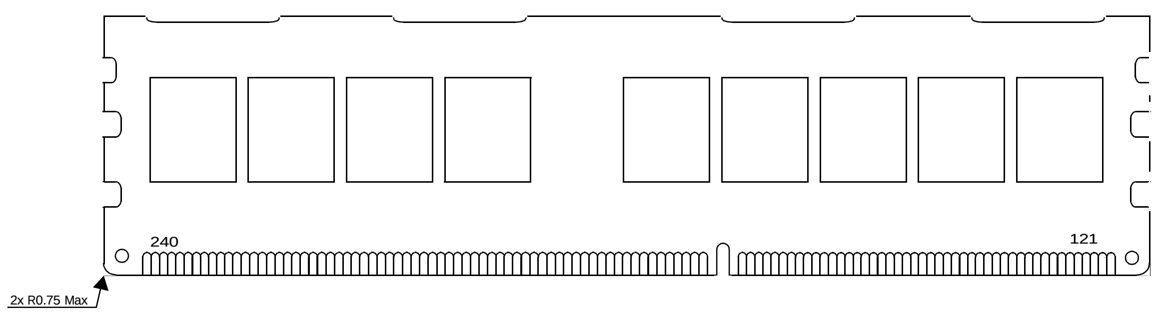
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512Mx72 - HMT351R7BFR8C

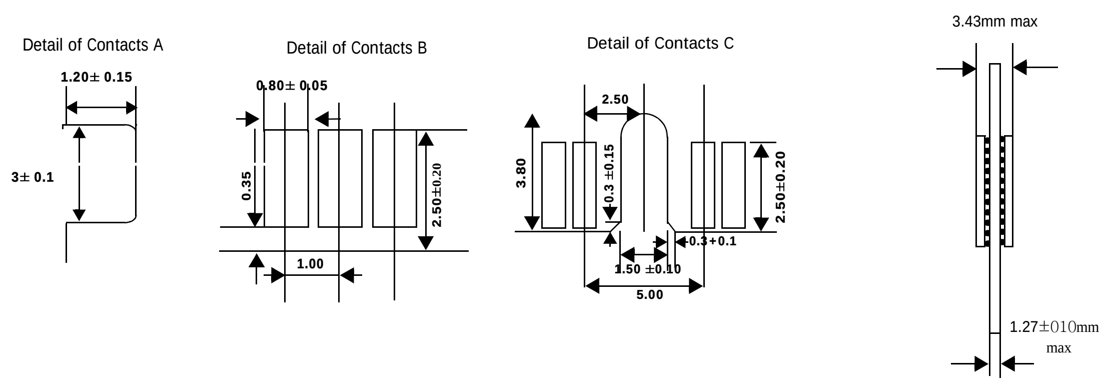
Front



Back



Side

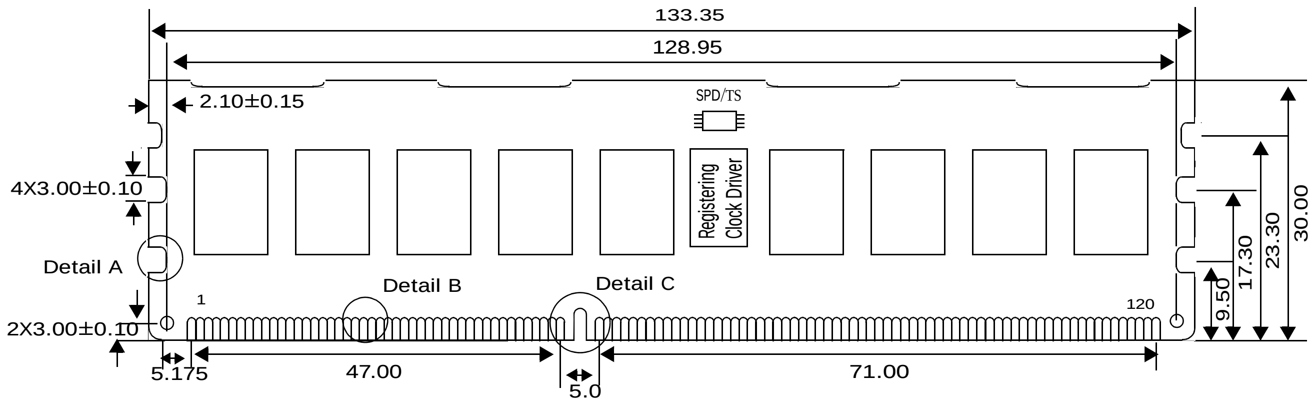


Note:
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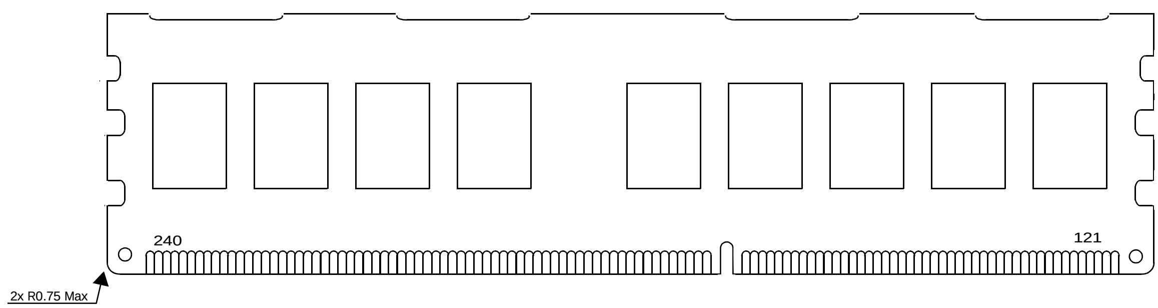
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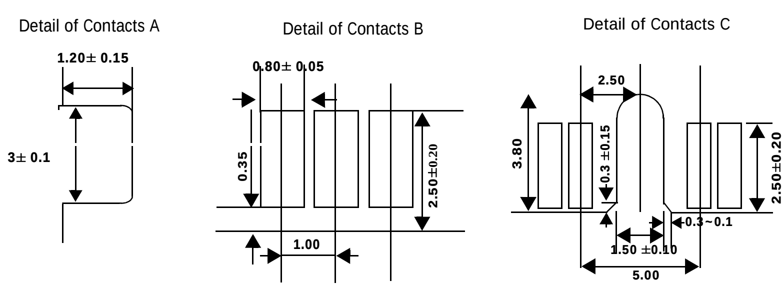
512Mx72 - HMT351R7BFR4C

Front

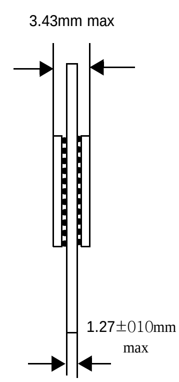


Back





Side



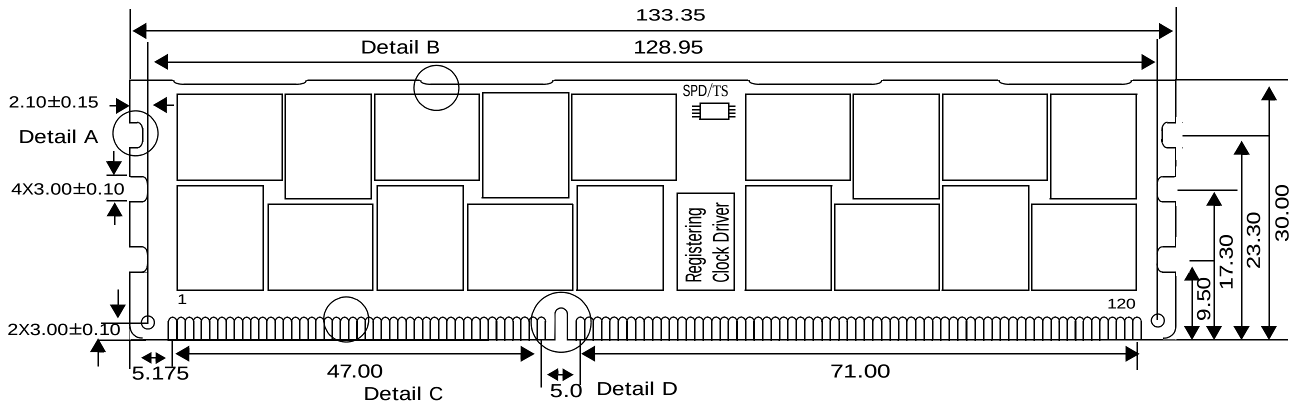
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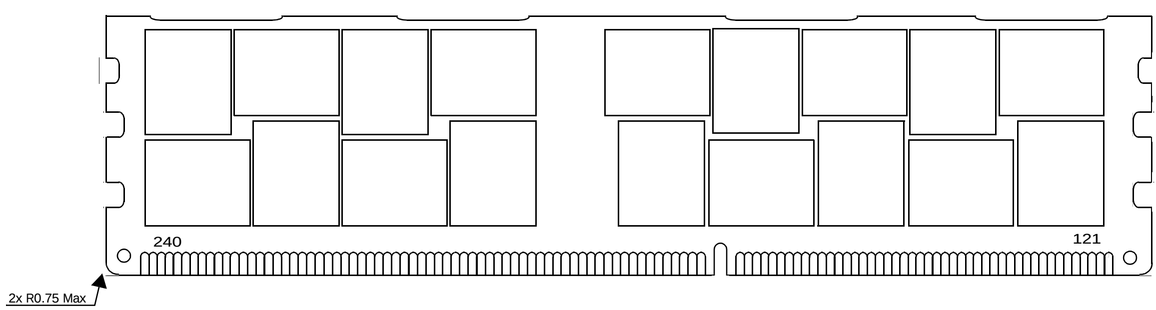
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1Gx72 - HMT31GR7BFR8C

Front

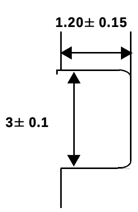


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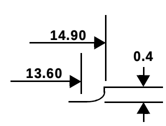


Side

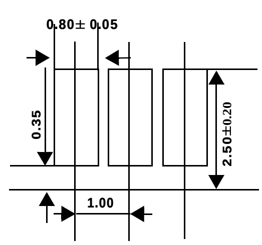
Detail of Contacts A



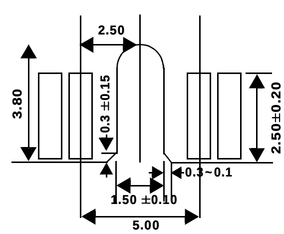
Detail of Contacts B



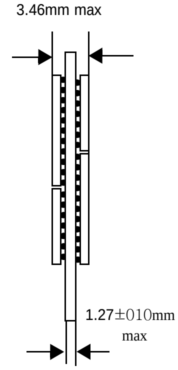
Detail of Contacts C



Detail of Contacts D



3.46mm max



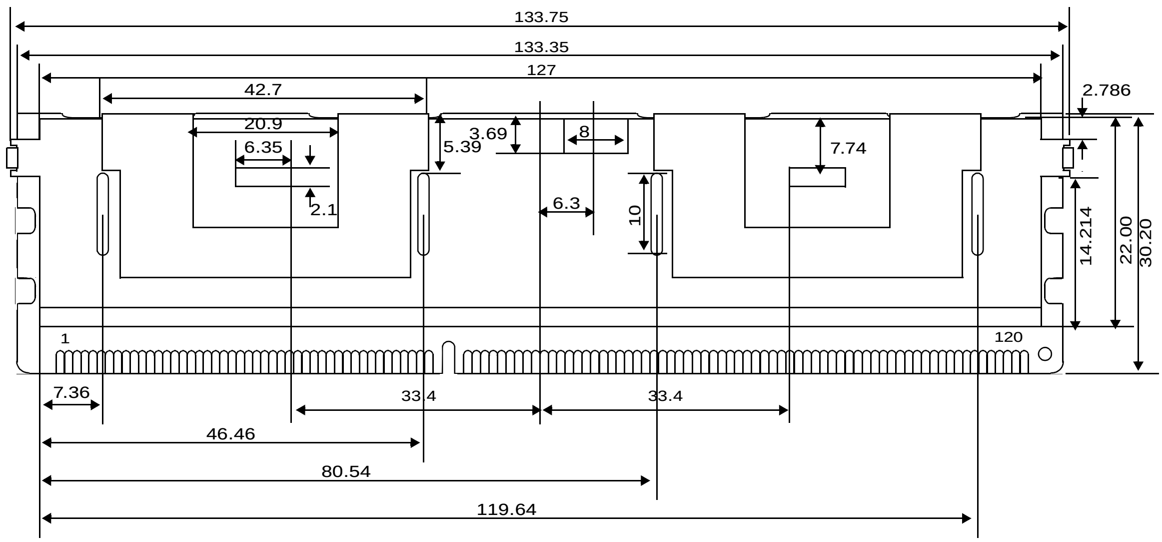
Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

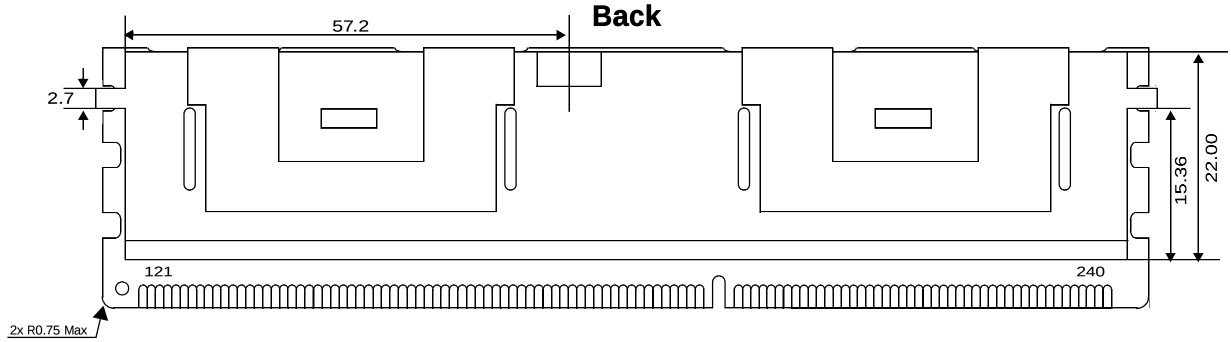
Units: millimeters

1Gx72 - HMT31GR7BFR8C - Heat Spreader

Front

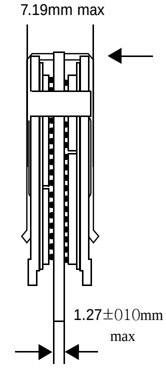


Back



Side

7.19mm max



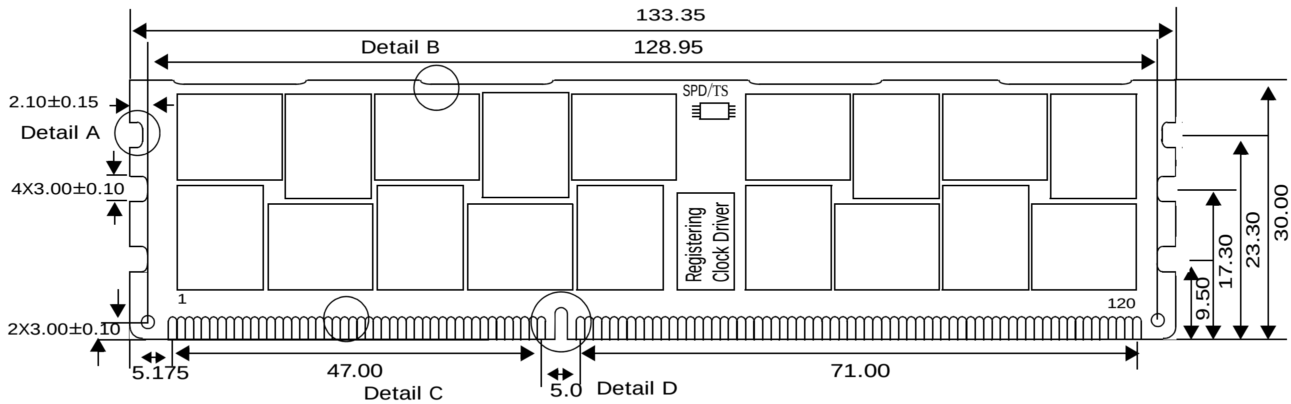
Note:

1. ± 0.13 tolerance on all dimensions unless otherwise stated.
2. In order to uninstall FDHS, please contact sales administrator.

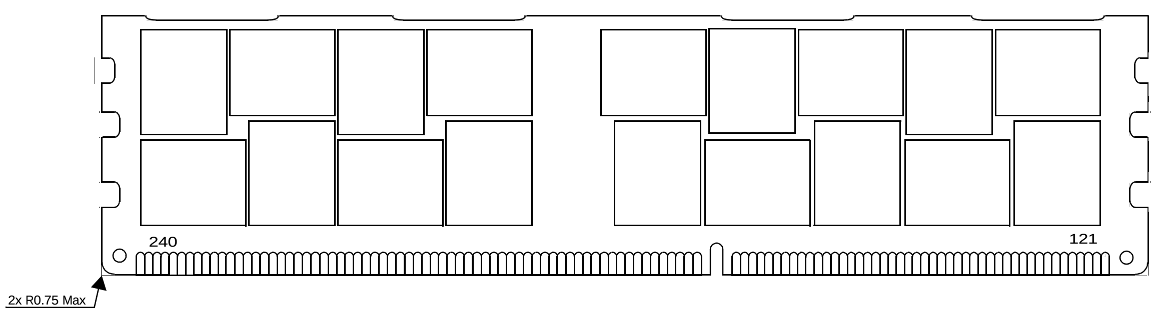
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1Gx72 - HMT31GR7BFR4C

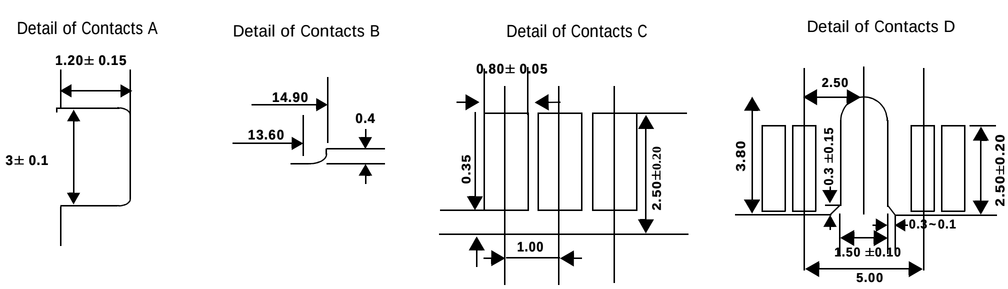
Front

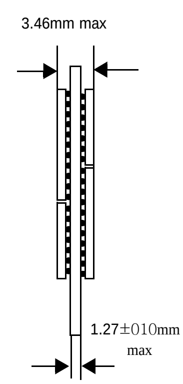


Back



Side



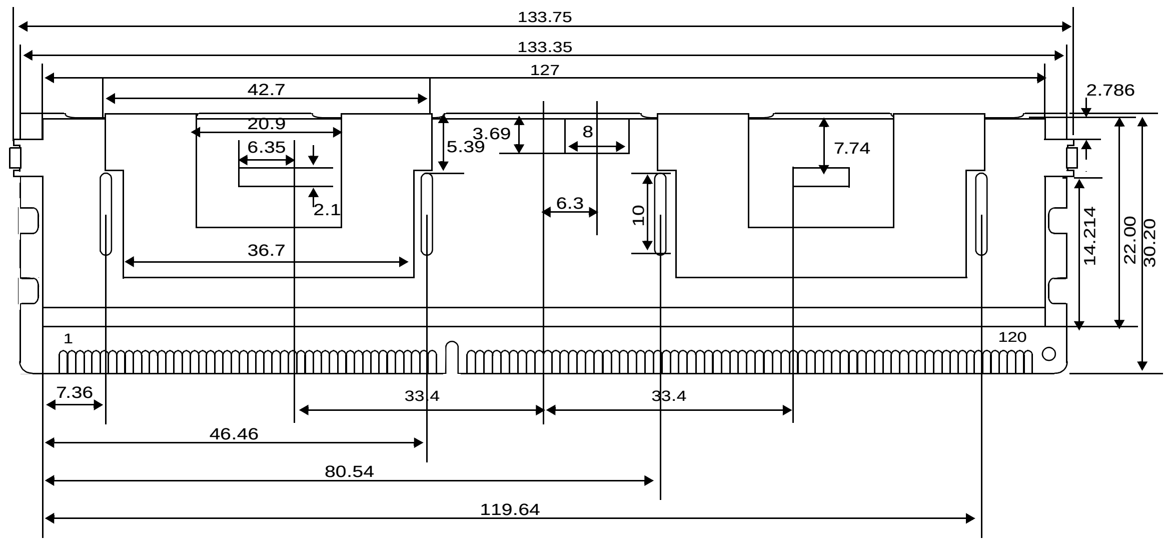


Note:
1. ±0.13 tolerance on all dimensions unless otherwise stated.

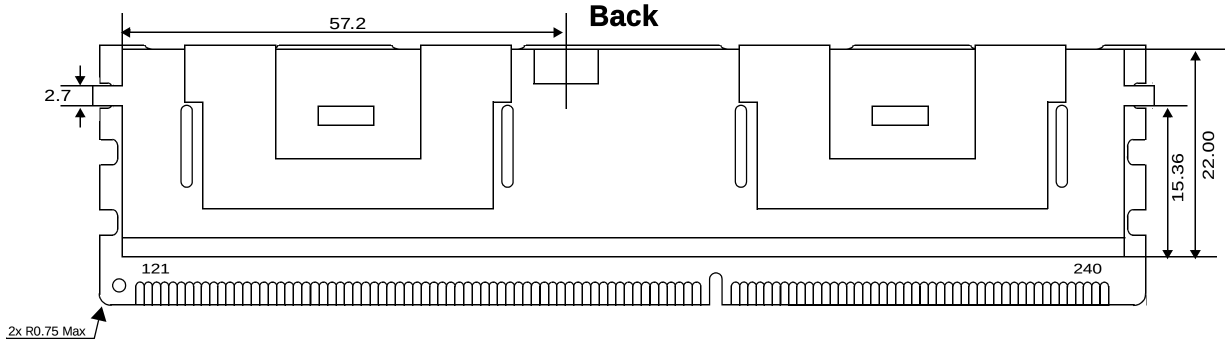
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1Gx72 - HMT31GR7BFR4C - Heat Spreader

Front

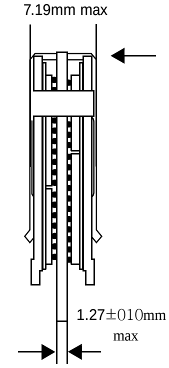


Back



Side

7.19mm max

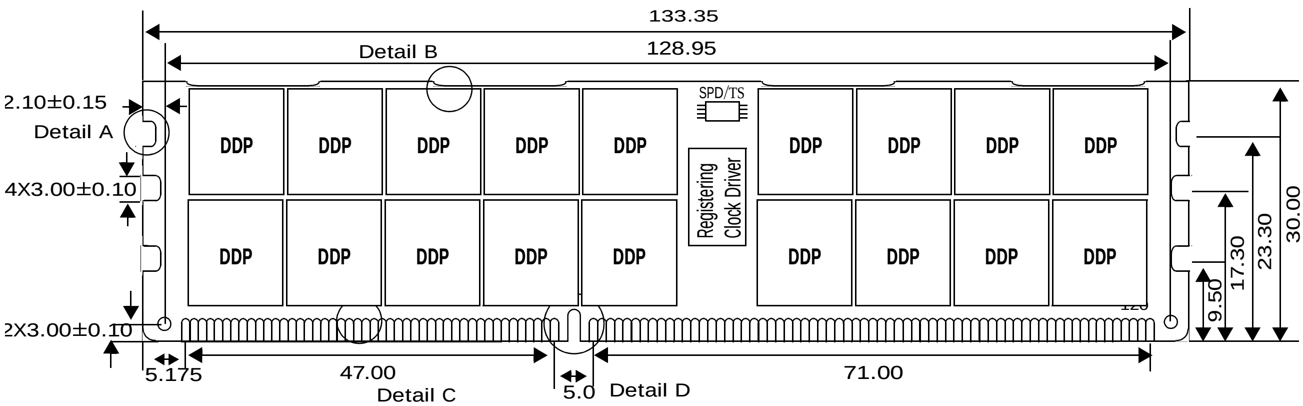


Note:
1. ± 0.13 tolerance on all dimensions unless otherwise stated.
2. In order to uninstall FDHS, please contact sales administrator.

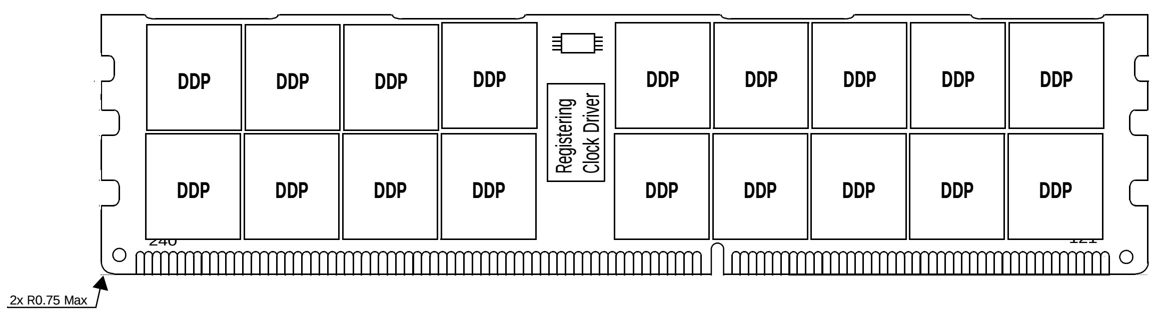
Units: millimeters

2Gx72 - HMT42GR7BMR4C

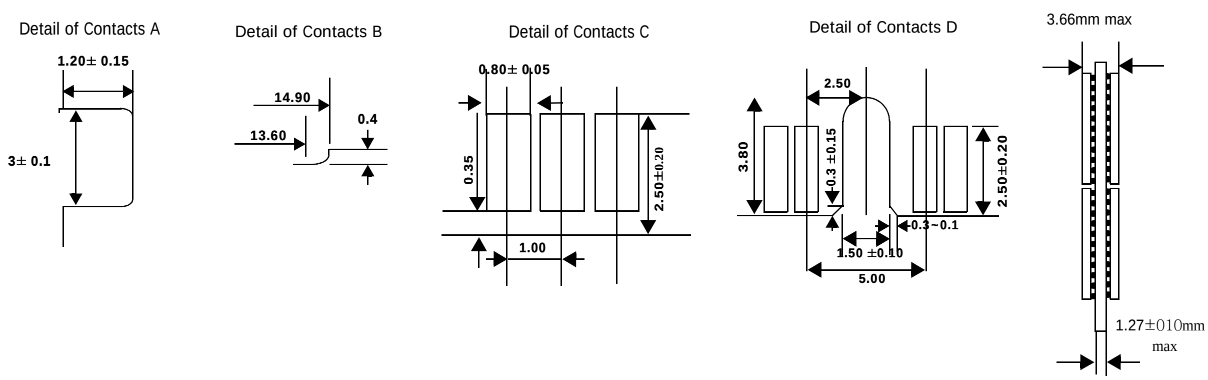
Front



Back



Side

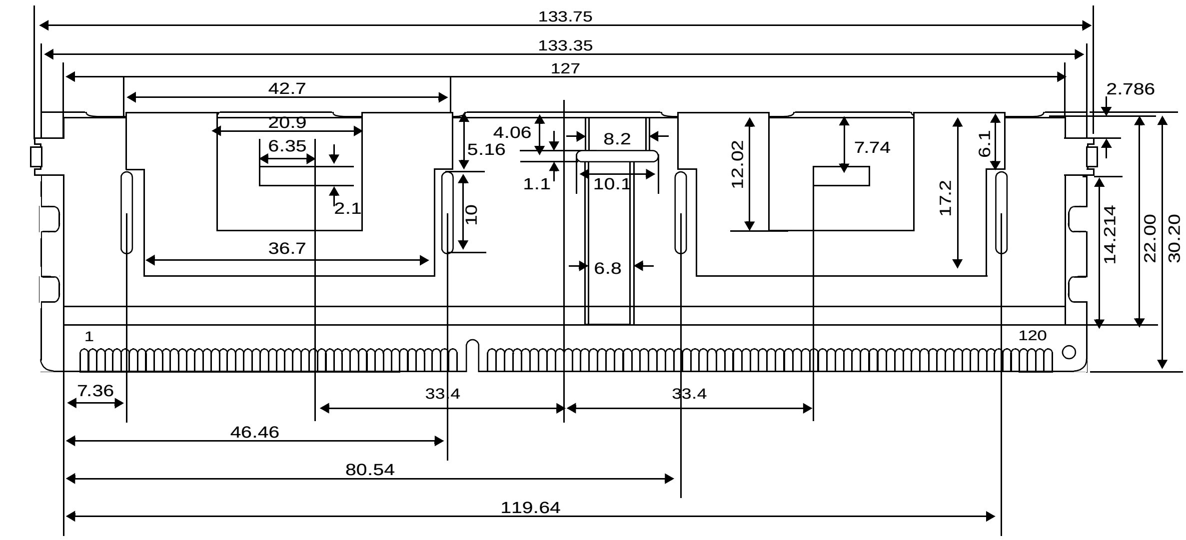


Note:
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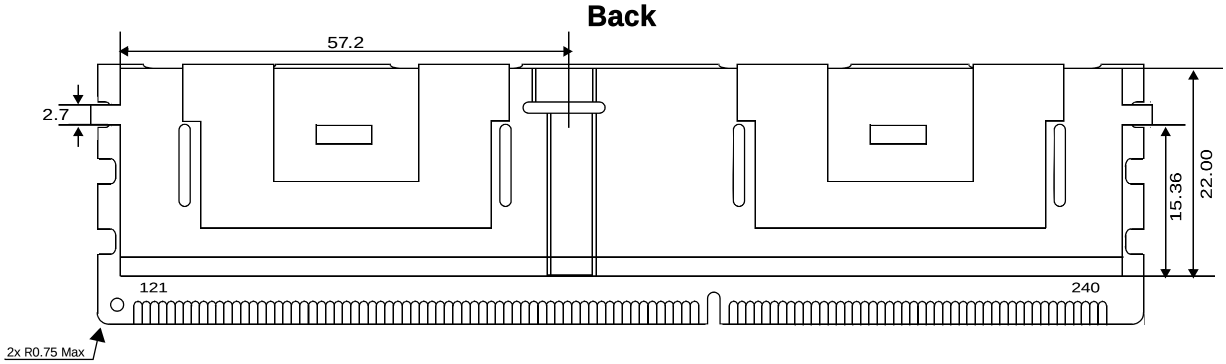
Units: millimeters

2Gx72 - HMT42GR7BMR4C - Heat Spreader

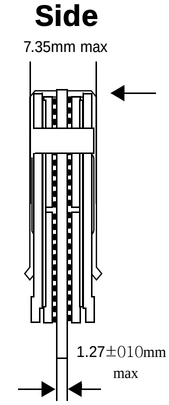
Front



Back



Side



Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.
2. In order to uninstall FDHS, please contact sales administrator.

Units: millimeters